

## PCB BOARD SIZE

4 Layers

244mmX 200mm

## On Board Header

CONN	Default	DESCRIPTION
JP1701	1-2	CMOS CLEAR
CN2902		HDMI SPDIF 1x4 pin
CN2903		Internal Speaker 2x4 pin
CN2901		Audio Front Panel 2x5 pin
CN601		HDT+ CONN (APU Debug)
CN5501		CPU FAN CONN 4 pin
CN5502		System FAN CONN 4 pin
CN6101		Internal USB 2.0
CN6102		Front USB 2.0
CN6202		Front USB 3.0
CN6801		ATX Power 24 pin
CN6802		Front Panel 2x8 pin
CN4201		ATX Power 4 pin
CN7101		Debug Port 2x7
CN7801		IR Reciever 1x3 pin
CN7802		GPIO 1x2 pin
CN7803		GPIO 1x2 pin

## XTAL Description

XTAL	Function	Frequency	Spec	Capacitance
X1702	FCH	25M	+-20ppm CL:12P	C1=C2=12pF
X1701	FCH	32.768K	+-20ppm CL:12.5P	C1=C2=18pF
X1901	LAN	25M	+-20ppm CL:12P	C1=C2=22pF
X6501	LAN	25M	+-20ppm CL:12P	C1=C2=22pF

FCH: HUDSON-D3 71.HUDD3.M01

SIO: IT8772E 71.08772.A0G

LAN: RTL8111E-VL 71.08111.J03

Audio Codec: ALC662-GR 71.00662.00G

## aParker

PROJECT CODE :48.3FU01.011

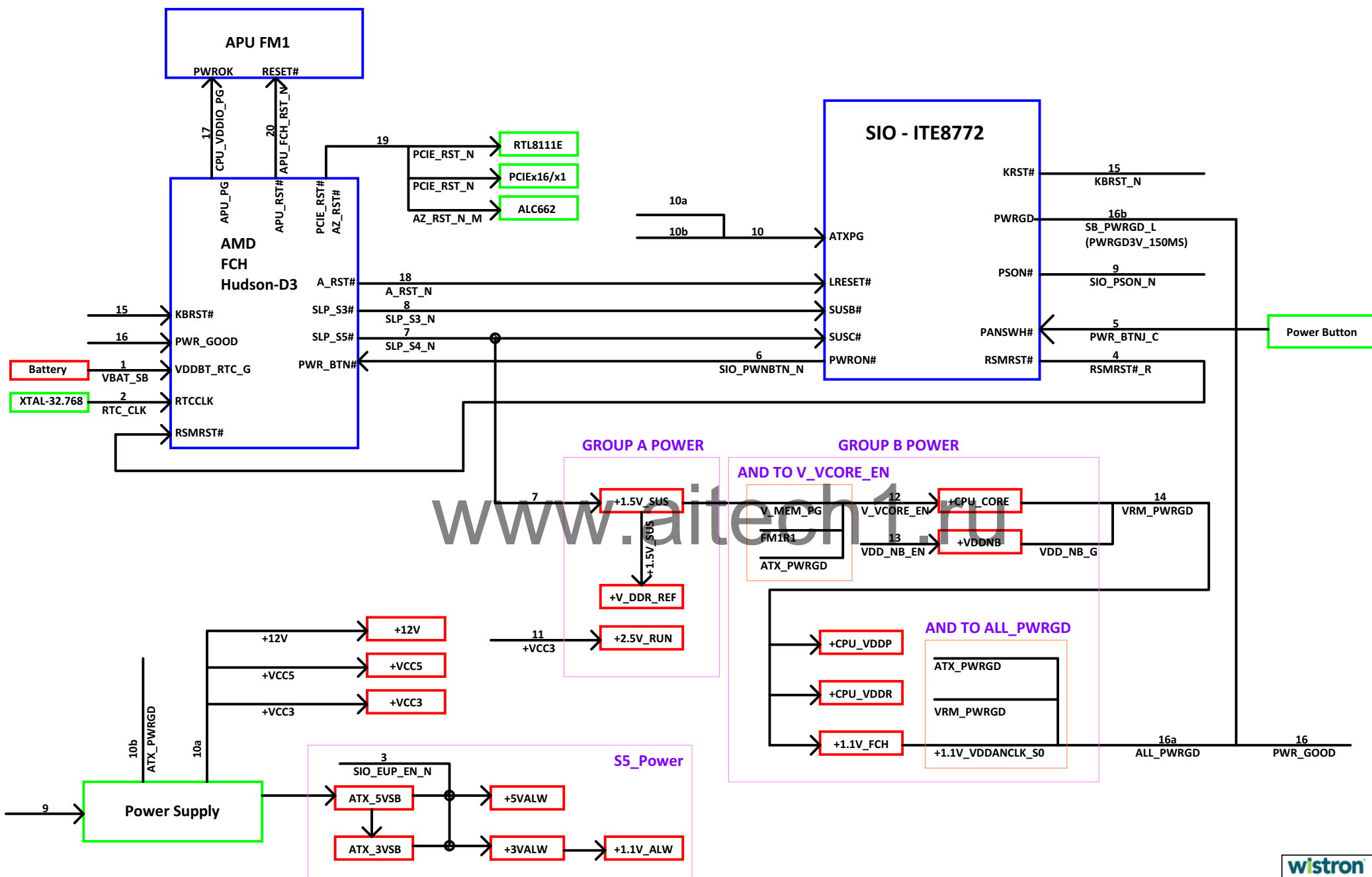
PCB Version: -1

PCB Number : 11005

PAGE	TITLE	Quantity
01	Cover Page	
02	Block Diagram	
03	Table of Content	
04	APU PCIE (1/6)	
05	APU DDR (2/6)	
06	APU Control&Debug (3/6)	
07	APU POWER (4/6)	
08	APU VSS (5/6)	
09	APU DISPLAY & MISC (6/6)	
10	(Reserve)	
11	(Reserve)	
12	(Reserve)	
13	DDR-DIMM0 Socket1	
14	DDR-DIMM1 Socket2	
15	DDR-DIMM0 Socket3	
16	DDR-DIMM1 Socket4	
17	HUDSON-M2 ACPI/PCI/CLK (1/6)	
18	HUDSON-M2 GPIO/USB (2/6)	
19	HUDSON-M2 SATA/HWM/SPI (3/6)	
20	HUDSON-M2 POWER (4/6)	
21	HUDSON-M2 STRAPPINGS (5/6)	
22	HUDSON-M2 VSS (6/6)	
23	(Reserve)	
24	(Reserve)	
25	(Reserve)	
26	(Reserve)	
27	(Reserve)	
28	(Reserve)	
29	Audio Codec (ALC662)	
30	(Reserve)	
31	(Reserve)	
32	(Reserve)	
33	(Reserve)	
34	(Reserve)	
35	(Reserve)	
36	(Reserve)	
37	(Reserve)	
38	(Reserve)	
39	(Reserve)	
40	DUAL POWER	
41	VREG : +3.3V_ALW&+5V_ALW	
42	VREG : +VCC_CORE	
43	VREG : +VDDNB	
44	VREG: +1.5V_SUS & +V_DDR_REF	
45	VREG: +VDDR& VDDP	
46	VREG: +1.1V_ALW/+1.2V_ALW	
47	(Reserve)	
48	LDO: 2.5V_RUN& +1.5V_RUN	
49	(Reserve)	
50	CRT Connector (VGA CONN)	
51	HDMI	

PAGE	TITLE	Quantity
52	(Reserve)	
53	(Reserve)	
54	(Reserve)	
55	FAN CONN	
56	HDD/ODD	
57	(Reserve)	
58	Microphone/Speaker/Audio	
59	RJ45+Transformer	
60	(Reserve)	
61	USB Port + Power Switch	
62	USB3.0 Connector	
63	(Reserve)	
64	(Reserve)	
65	(Reserve)	
66	(Reserve)	
67	(Reserve)	
68	LED/Button	
69	Keyboard/Touch pad	
70	(Reserve)	
71	Serial port/JTAG/Debug port	
72	(Reserve)	
73	(Reserve)	
74	(Reserve)	
75	Express Card(x16 and x1slot)	
76	(Reserve)	
77	(Reserve)	
78	SIO (ITE8772E)	
79	(Reserve)	
80	(Reserve)	
81	Screw Holes, Springs, BOSS	
82	(Reserve)	
83	(Reserve)	
84	(Reserve)	
85	(Reserve)	
86	(Reserve)	
87	(Reserve)	
88	(Reserve)	
89	(Reserve)	
90	(Reserve)	
91	(Reserve)	
92	(Reserve)	
93	(Reserve)	
94	(Reserve)	
95	(Reserve)	
96	Power Block Diagram	
97	(Reserve)	
98	(Reserve)	
99	(Reserve)	





## PCIEX16

75 P\_GFX\_RXP[0..15] <<<<  
75 P\_GFX\_RXN[0..15] <<<<  
75 C\_GFX\_TXP[0..15] <<<<  
75 C\_GFX\_TXN[0..15] <<<<

## UMI TO FCH

17 PCIE\_NB\_RXP[0..3] <<<<  
17 PCIE\_NB\_RXN[0..3] <<<<  
17 PCIE\_NB\_TXP[0..3] <<<<  
17 PCIE\_NB\_TXN[0..3] <<<<

## PCIEX1

75 PCIE\_C\_RXP1 <<<<  
75 PCIE\_C\_RXN1 <<<<  
75 C\_GPP\_TXP1 <<<<  
75 C\_GPP\_TXN1 <<<<

## LAN

65 HSO\_BLAN\_DP5 <<<<  
65 HSO\_BLAN\_DN5 <<<<  
65 HSI\_BLAN\_DP5 <<<<  
65 HSI\_BLAN\_DN5 <<<<

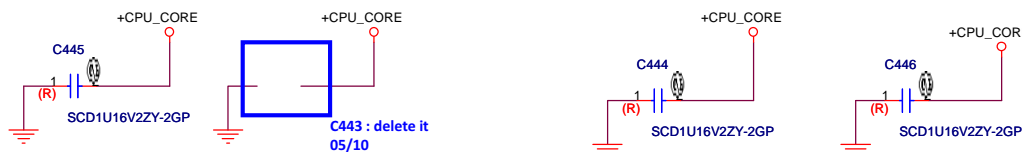
Follow Nadia, connect to LAN

Follow Nadia, connect to LAN

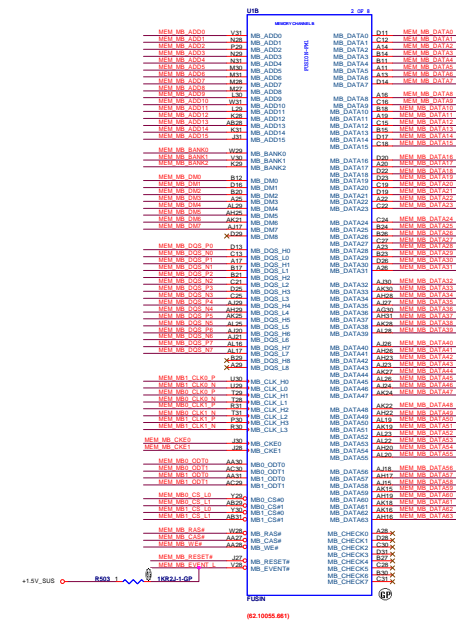
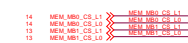
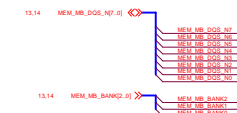
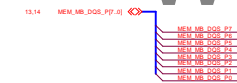
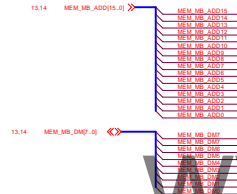
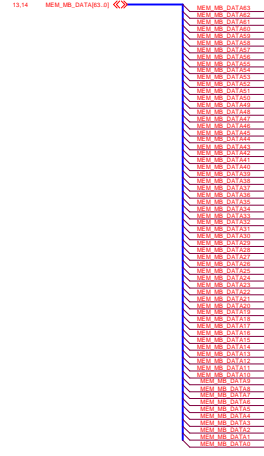
## UMI TO FCH

P\_ZVDDP, P\_ZVSS set the drive strength for the DisplayPort Main Link signals

Added EMI CAP 0404

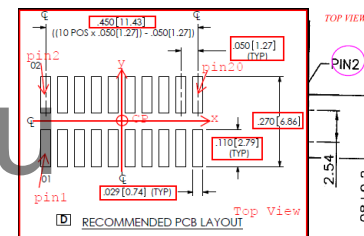


<b>wistron</b>		<b>Wistron Incorporated</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd	
		Hsichih, Taipei Hsien	
Title			
<b>APU PCIE</b>			
Size	Document Number		Rev
B	<b>Parker</b>		-1
Date:	Thursday, July 14, 2011		Sheet 4 of 99



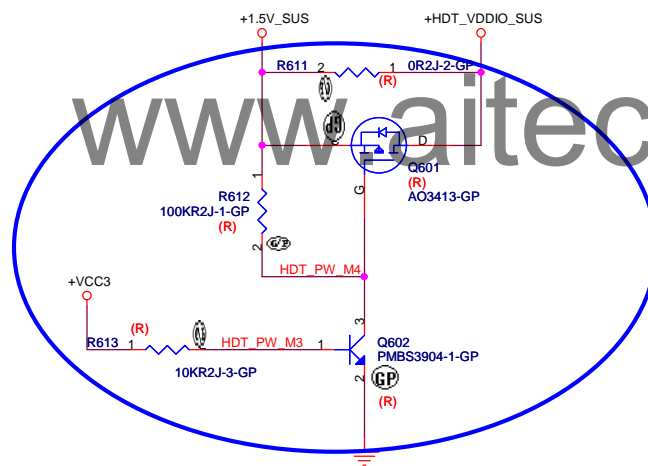
CHECK[0:8]AMD- FM1 does not support ECC.  
The CRB layout engineers always route all signals

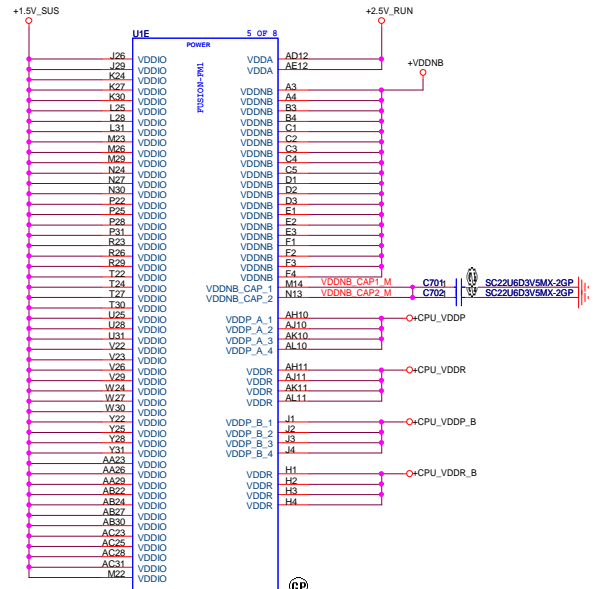
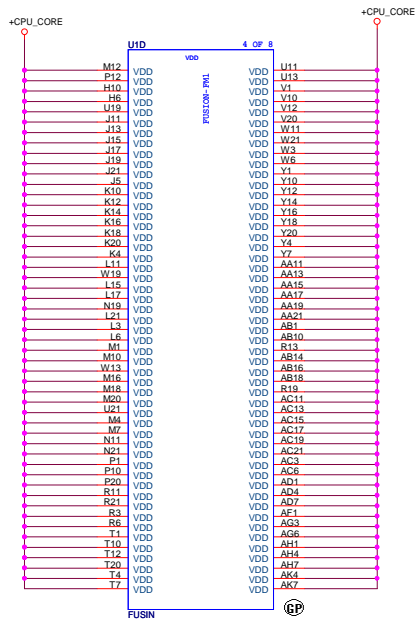




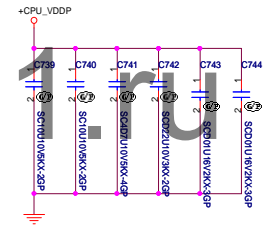
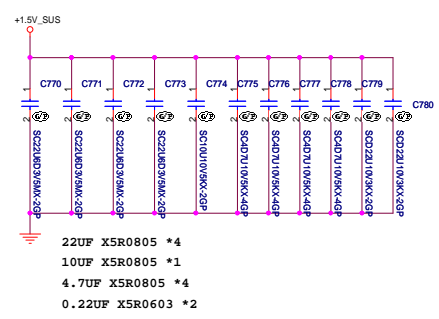
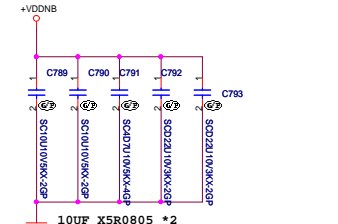
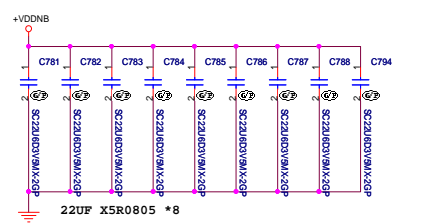
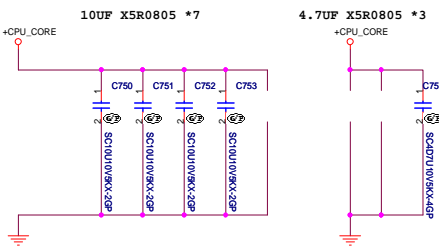
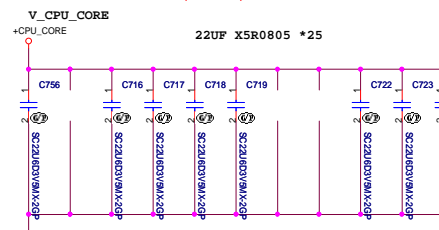
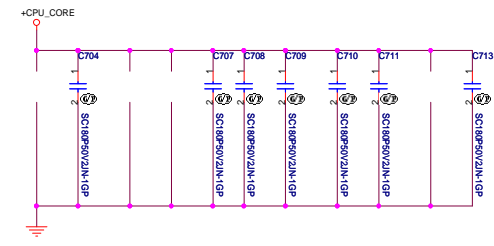
9 APU\_TRST  
9 APU\_TCK  
9 APU\_TMS  
9 APU\_TDI  
9 APU\_TDO  
9 APU\_DBRDY  
9 APU\_DBREQ

9 TEST19\_M  
9 TEST18\_M

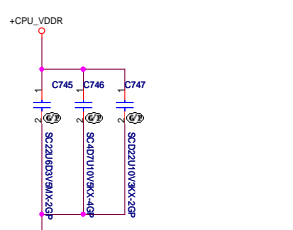




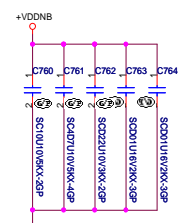
# EMC CAP BOTTOM



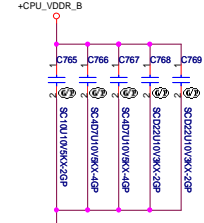
- 10UF X5R0805 \*2
- 4.7UF X5R0805 \*1
- 0.22UF X5R0603 \*1
- 0.01UF X7R0402 \*2



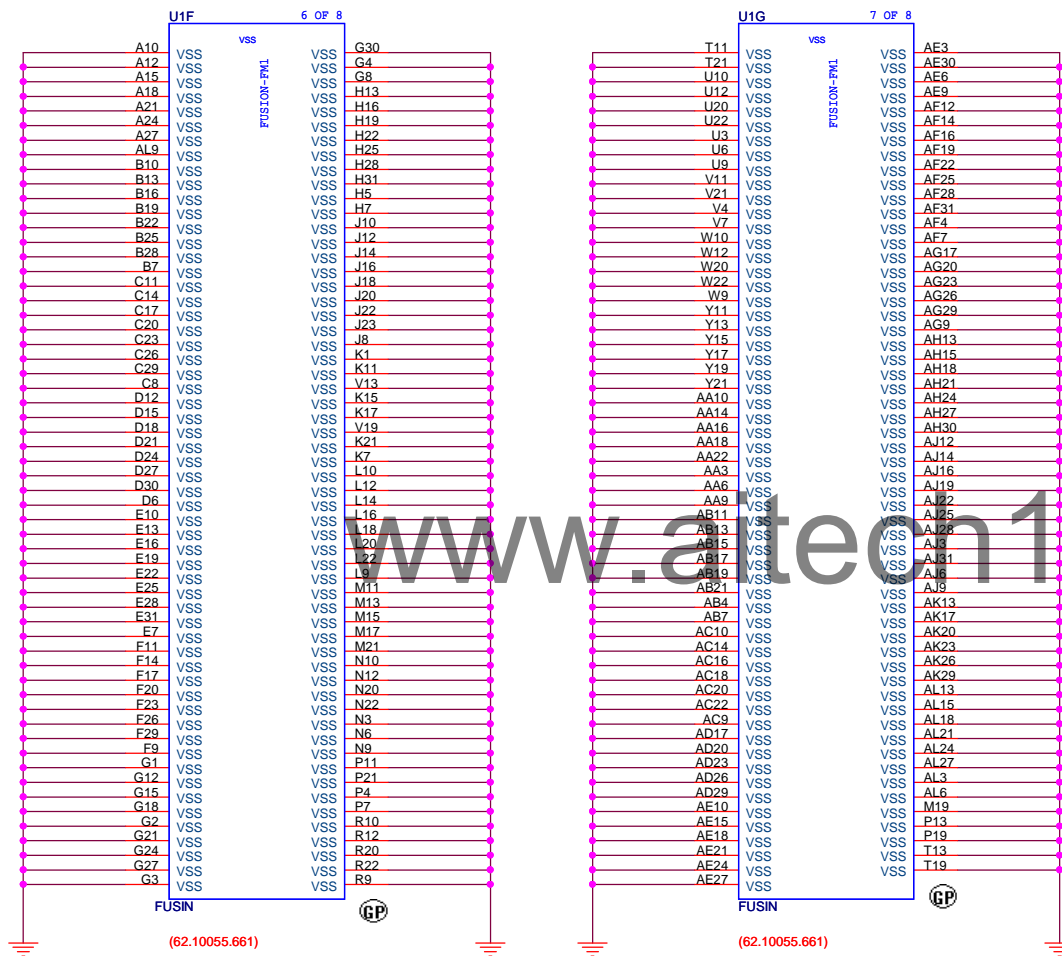
- 22UF X5R0805 \*1
- 4.7UF X5R0805 \*1
- 0.22UF X5R0603 \*1



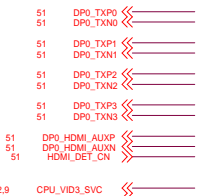
- 10UF X5R0805 \*1
- 4.7UF X5R0805 \*1
- 0.22UF X5R0603 \*1
- 0.01UF X7R0402 \*2



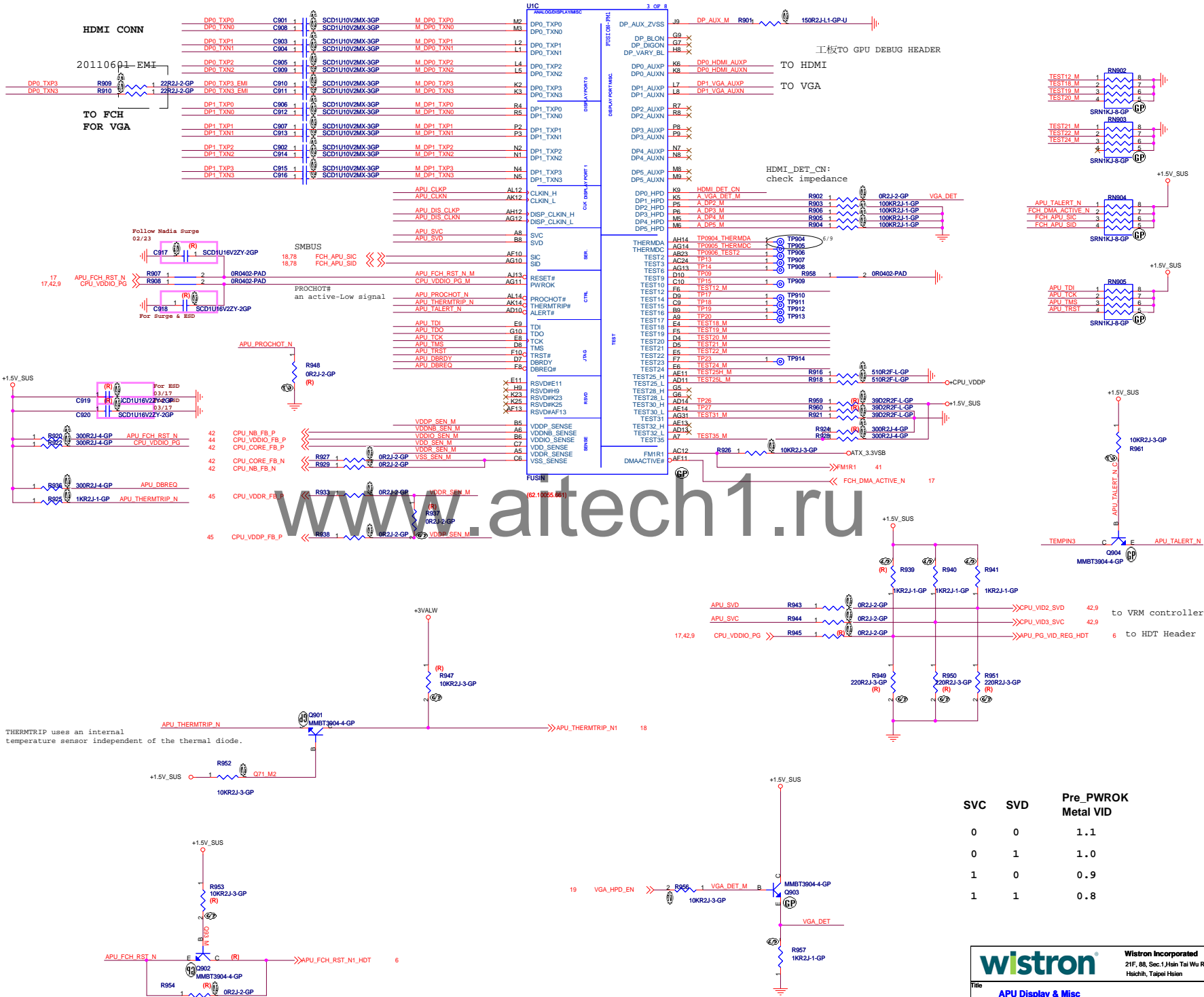
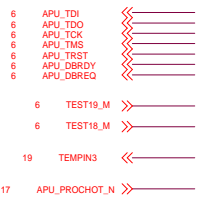
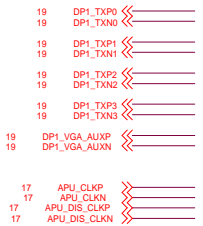
- 10UF X5R0805 \*1
- 4.7UF X5R0805 \*2
- 0.22UF X5R0603 \*2



## HDMI



## VGA




SVC	SVD	Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

TBD

www.aitech1.ru

TBD

www.aitech1.ru

		<b>Wistron Incorporated</b> 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title Reserve			
Size B	Document Number Parker		Rev -1
Date:	Friday, May 13, 2011		Sheet 11 of 99

**TBD**

[www.aitech1.ru](http://www.aitech1.ru)



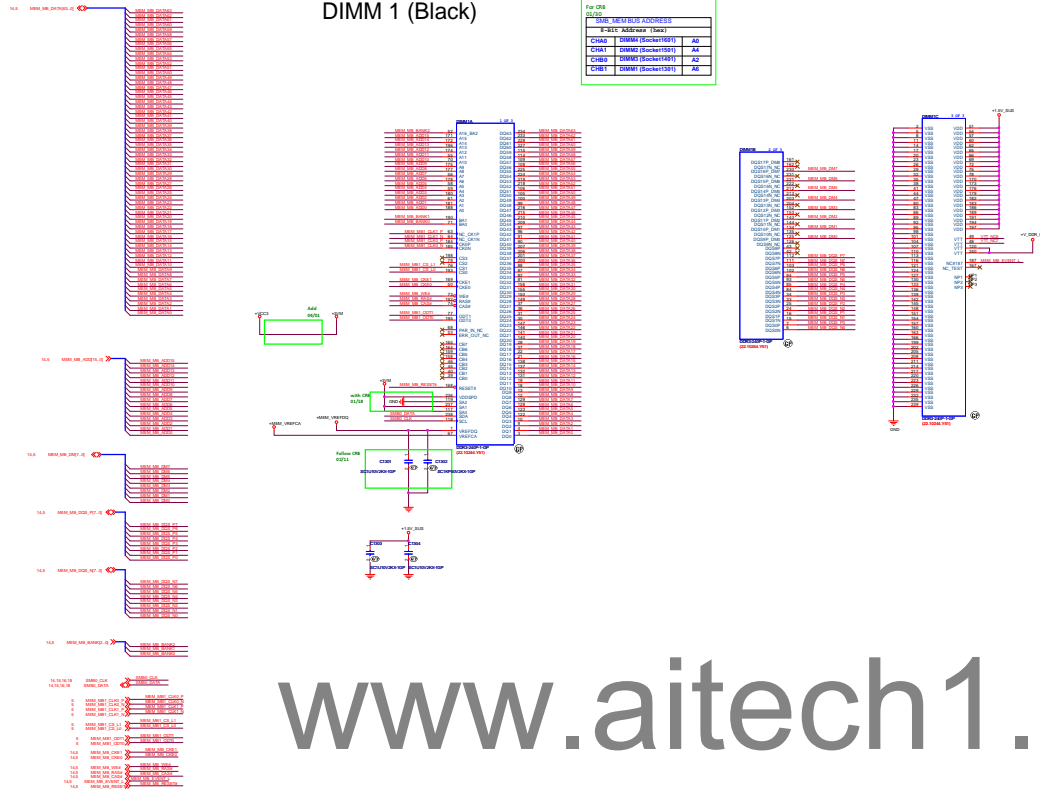
**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			Reserve
Size	Document Number		Rev
B	Parker		-1
Date:	Friday, May 13, 2011		Sheet 12 of 99

MEM\_B1

# DIMM 1 (Black)

For DIMM			
E-EEP ADDRESS			
Chip	Address	Value	
CH00	00000000	00	A0
CH01	00000000	00	A0
CH02	00000000	00	A0
CH03	00000000	00	A0



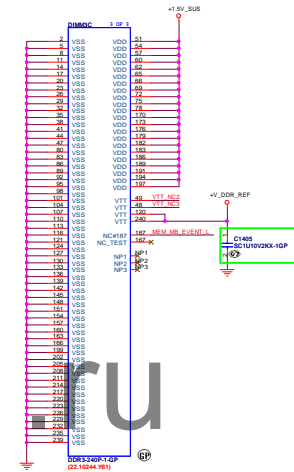
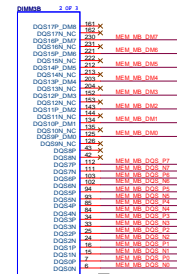
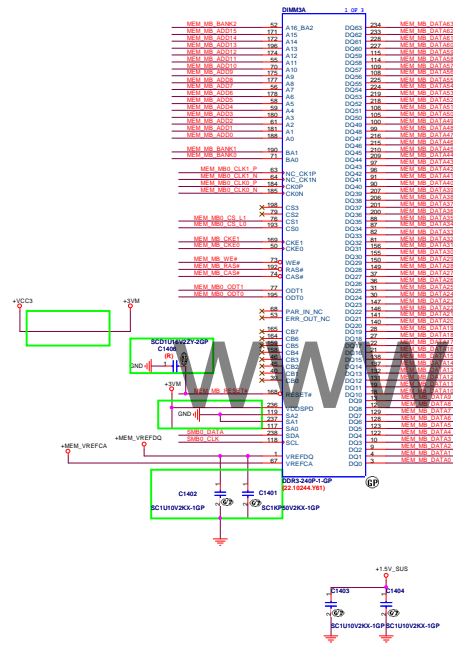
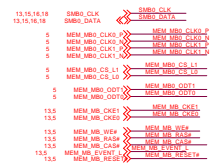
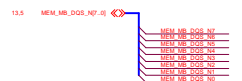
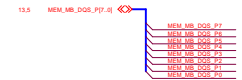
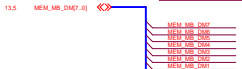
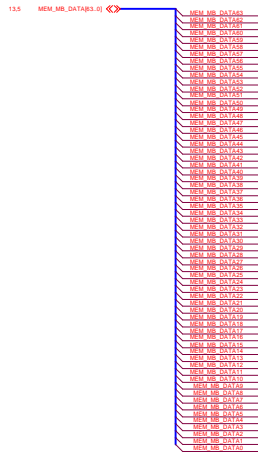
www.aitech1.ru

MEM\_B0

## DIMM 3 (Blue)

For CRB  
01/20

SMB MEM BUS ADDRESS		
8-bit Address (hex)		
CHA0	DIMM4 (Socket1601)	A0
CHA1	DIMM2 (Socket1501)	A4
CHB0	DIMM3 (Socket1401)	A2
CHB1	DIMM1 (Socket1301)	A6



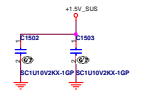
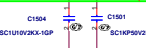
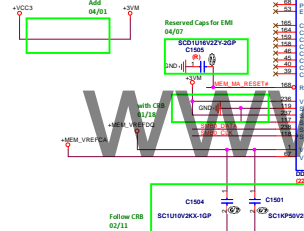
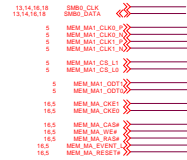
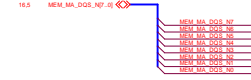
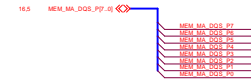
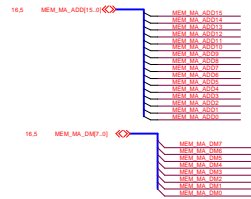
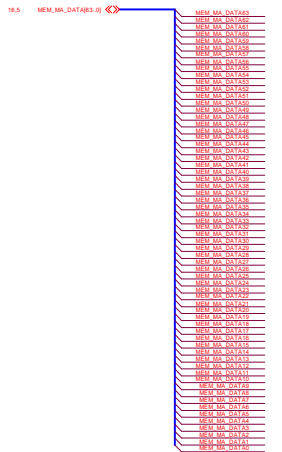
MEM\_A1

## DIMM 2 (Black)

Notes 22.10244.K41(Blue) and  
22.10244.K31(Black)  
Tyco 22.10244.K21(Blue) and  
22.10244.K51(Black)

For CRB

SMB_MEM BUS ADDRESS		
8-Bit Address (hex)		
CHA0	DIMM4 (Socket1601)	A0
CHA1	DIMM2 (Socket1501)	A4
CHB0	DIMM3 (Socket1401)	A2
CHB1	DIMM1 (Socket1301)	A6





# UMI to FCH

4 POE\_NB\_RXP0\_0  
5 POE\_NB\_RXP0\_1  
4 POE\_NB\_TXP0\_0  
4 POE\_NB\_TXP0\_1

# CLOCK

8 APU\_D0S\_CLKP  
9 APU\_D0S\_CLKN  
9 APU\_CLKP  
9 APU\_CLKN  
75 POE18\_CLKP  
75 POE18\_CLKN  
75 POE1X1\_C\_CLKP  
75 POE1X1\_C\_CLKN  
65 CLK\_BLAN\_DP  
65 CLK\_BLAN\_DN

# STRAPS

21 PCI\_AD03  
21 PCI\_AD04  
21 PCI\_AD05  
21 PCI\_AD06  
21 PCI\_AD07

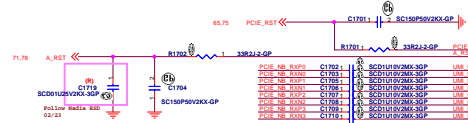
# LPC

7178 LAD0\_F0H0  
7178 LAD0\_F0H1  
7178 LAD0\_F0H2  
7178 LAD0\_F0H3  
7178 LFRAME\_F0H0  
7178 LFRAME\_F0H1  
7178 LFRAME\_F0H2  
7178 LFRAME\_F0H3

# OTHERS

9 APU\_F0H\_RST\_N  
425 FCH\_D0M\_ACTIVE\_N  
4270 HT\_CPU\_PWR02\_R  
78 SERIRQ  
21 RTC\_CLK  
9 APU\_PROCHOT\_N  
16 FCH\_PROCHOT  
18 DL\_N0

TO PCIEX1, X4, X16, LAN CHIP



UMI

Changed connect to +1.1V\_VDDANCLK\_S0

04/08

+1.1V\_VDDANCLK\_S0

04/08

TO PCIEX4

Changed connect to +1.1V\_VDDANCLK\_S0

04/08

+1.1V\_VDDANCLK\_S0

04/08

TO CPU

For internal clock generator, NOISE USE

2010601

TO CPU

TO PCIEX16

FOR GRAPHIC CARD

02/11

TO CPU

TO PCIEX1

TO PCIEX4

TO LAN

DOUBLE CHECK!!! CRB HAS NOT

02/11

Reserved CAPs for EMI

04/08

FOLLOW NADIA, CRB RESERVE FOR LAN

02/11

APERTURE

02/11

XTAL\_32M\_P0H0

XTAL\_32M\_P0H1

XTAL\_32M\_P0H2

XTAL\_32M\_P0H3

XTAL\_32M\_P0H4

XTAL\_32M\_P0H5

XTAL\_32M\_P0H6

XTAL\_32M\_P0H7

XTAL\_32M\_P0H8

XTAL\_32M\_P0H9

XTAL\_32M\_P0H10

XTAL\_32M\_P0H11

XTAL\_32M\_P0H12

XTAL\_32M\_P0H13

XTAL\_32M\_P0H14

XTAL\_32M\_P0H15

XTAL\_32M\_P0H16

XTAL\_32M\_P0H17

XTAL\_32M\_P0H18

XTAL\_32M\_P0H19

XTAL\_32M\_P0H20

XTAL\_32M\_P0H21

XTAL\_32M\_P0H22

XTAL\_32M\_P0H23

XTAL\_32M\_P0H24

XTAL\_32M\_P0H25

XTAL\_32M\_P0H26

XTAL\_32M\_P0H27

XTAL\_32M\_P0H28

XTAL\_32M\_P0H29

XTAL\_32M\_P0H30

XTAL\_32M\_P0H31

XTAL\_32M\_P0H32

XTAL\_32M\_P0H33

XTAL\_32M\_P0H34

XTAL\_32M\_P0H35

XTAL\_32M\_P0H36

XTAL\_32M\_P0H37

XTAL\_32M\_P0H38

XTAL\_32M\_P0H39

XTAL\_32M\_P0H40

XTAL\_32M\_P0H41

XTAL\_32M\_P0H42

XTAL\_32M\_P0H43

XTAL\_32M\_P0H44

XTAL\_32M\_P0H45

XTAL\_32M\_P0H46

XTAL\_32M\_P0H47

XTAL\_32M\_P0H48

XTAL\_32M\_P0H49

XTAL\_32M\_P0H50

XTAL\_32M\_P0H51

XTAL\_32M\_P0H52

XTAL\_32M\_P0H53

XTAL\_32M\_P0H54

XTAL\_32M\_P0H55

XTAL\_32M\_P0H56

XTAL\_32M\_P0H57

XTAL\_32M\_P0H58

XTAL\_32M\_P0H59

XTAL\_32M\_P0H60

XTAL\_32M\_P0H61

XTAL\_32M\_P0H62

XTAL\_32M\_P0H63

XTAL\_32M\_P0H64

XTAL\_32M\_P0H65

XTAL\_32M\_P0H66

XTAL\_32M\_P0H67

XTAL\_32M\_P0H68

XTAL\_32M\_P0H69

XTAL\_32M\_P0H70

XTAL\_32M\_P0H71

XTAL\_32M\_P0H72

XTAL\_32M\_P0H73

XTAL\_32M\_P0H74

XTAL\_32M\_P0H75

XTAL\_32M\_P0H76

XTAL\_32M\_P0H77

XTAL\_32M\_P0H78

XTAL\_32M\_P0H79

XTAL\_32M\_P0H80

XTAL\_32M\_P0H81

XTAL\_32M\_P0H82

XTAL\_32M\_P0H83

XTAL\_32M\_P0H84

XTAL\_32M\_P0H85

XTAL\_32M\_P0H86

XTAL\_32M\_P0H87

XTAL\_32M\_P0H88

XTAL\_32M\_P0H89

XTAL\_32M\_P0H90

XTAL\_32M\_P0H91

XTAL\_32M\_P0H92

XTAL\_32M\_P0H93

XTAL\_32M\_P0H94

XTAL\_32M\_P0H95

XTAL\_32M\_P0H96

XTAL\_32M\_P0H97

XTAL\_32M\_P0H98

XTAL\_32M\_P0H99

XTAL\_32M\_P0H100

XTAL\_32M\_P0H101

XTAL\_32M\_P0H102

XTAL\_32M\_P0H103

XTAL\_32M\_P0H104

XTAL\_32M\_P0H105

XTAL\_32M\_P0H106

XTAL\_32M\_P0H107

XTAL\_32M\_P0H108

XTAL\_32M\_P0H109

XTAL\_32M\_P0H110

XTAL\_32M\_P0H111

XTAL\_32M\_P0H112

XTAL\_32M\_P0H113

XTAL\_32M\_P0H114

XTAL\_32M\_P0H115

XTAL\_32M\_P0H116

XTAL\_32M\_P0H117

XTAL\_32M\_P0H118

XTAL\_32M\_P0H119

XTAL\_32M\_P0H120

XTAL\_32M\_P0H121

XTAL\_32M\_P0H122

XTAL\_32M\_P0H123

XTAL\_32M\_P0H124

XTAL\_32M\_P0H125

XTAL\_32M\_P0H126

XTAL\_32M\_P0H127

XTAL\_32M\_P0H128

XTAL\_32M\_P0H129

XTAL\_32M\_P0H130

XTAL\_32M\_P0H131

XTAL\_32M\_P0H132

XTAL\_32M\_P0H133

XTAL\_32M\_P0H134

XTAL\_32M\_P0H135

XTAL\_32M\_P0H136

XTAL\_32M\_P0H137

XTAL\_32M\_P0H138

XTAL\_32M\_P0H139

XTAL\_32M\_P0H140

XTAL\_32M\_P0H141

XTAL\_32M\_P0H142

XTAL\_32M\_P0H143

XTAL\_32M\_P0H144

XTAL\_32M\_P0H145

XTAL\_32M\_P0H146

XTAL\_32M\_P0H147

XTAL\_32M\_P0H148

XTAL\_32M\_P0H149

XTAL\_32M\_P0H150

XTAL\_32M\_P0H151

XTAL\_32M\_P0H152

XTAL\_32M\_P0H153

XTAL\_32M\_P0H154

XTAL\_32M\_P0H155

XTAL\_32M\_P0H156

XTAL\_32M\_P0H157

XTAL\_32M\_P0H158

XTAL\_32M\_P0H159

XTAL\_32M\_P0H160

XTAL\_32M\_P0H161

XTAL\_32M\_P0H162

XTAL\_32M\_P0H163

XTAL\_32M\_P0H164

XTAL\_32M\_P0H165

XTAL\_32M\_P0H166

XTAL\_32M\_P0H167

XTAL\_32M\_P0H168

XTAL\_32M\_P0H169

XTAL\_32M\_P0H170

XTAL\_32M\_P0H171

XTAL\_32M\_P0H172

XTAL\_32M\_P0H173

XTAL\_32M\_P0H174

XTAL\_32M\_P0H175

XTAL\_32M\_P0H176

XTAL\_32M\_P0H177

XTAL\_32M\_P0H178

XTAL\_32M\_P0H179

XTAL\_32M\_P0H180

XTAL\_32M\_P0H181

XTAL\_32M\_P0H182

XTAL\_32M\_P0H183

XTAL\_32M\_P0H184

XTAL\_32M\_P0H185

XTAL\_32M\_P0H186

XTAL\_32M\_P0H187

XTAL\_32M\_P0H188

XTAL\_32M\_P0H189

XTAL\_32M\_P0H190

XTAL\_32M\_P0H191

XTAL\_32M\_P0H192

XTAL\_32M\_P0H193

XTAL\_32M\_P0H194

XTAL\_32M\_P0H195

XTAL\_32M\_P0H196

XTAL\_32M\_P0H197

XTAL\_32M\_P0H198

XTAL\_32M\_P0H199

XTAL\_32M\_P0H200

XTAL\_32M\_P0H201

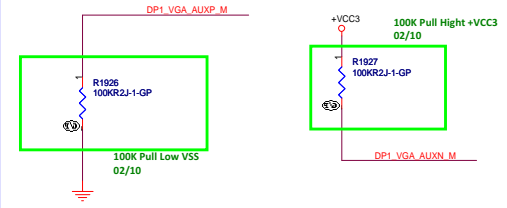
XTAL\_32M\_P0H202

XTAL\_32M\_P0H203

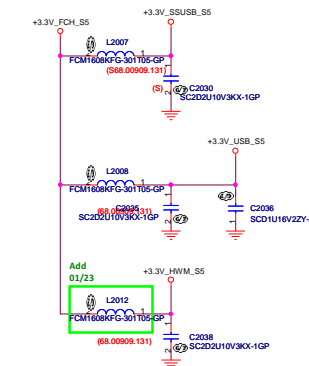
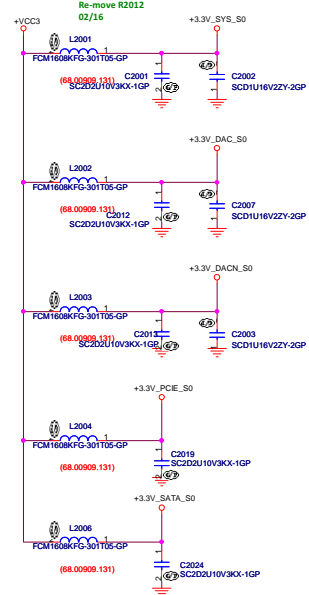
XTAL\_32M\_P0H204



TO SATA 3.0CONN

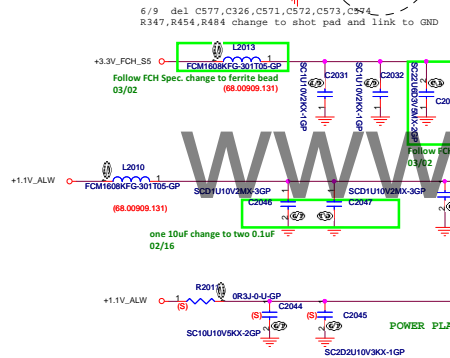


+3VALW  
+3V\_FCH\_S5  
3.3V\_XXX\_S5  
1.1V\_XXX\_S5  
3.3V\_XXX\_S0  
1.1V\_XXX\_S0



3.3V\_SSUSB\_S0  
USB3.0 WAKE=> 3.3V\_SSUSB\_S5  
NONE=> 3.3V\_SSUSB\_S0

WAKE ON LAN=> XXX\_S5  
NONE=>XXX\_S0



POWER PLANE

POWER PLANE

POWER PLANE

POWER PLANE

POWER PLANE

POWER PLANE

POWER PLANE

POWER PLANE

POWER PLANE

HUDSON-D3-GP  
(S71,HUD03.M02,F71,HUD02.M03)

POWER PLANE

POWER PLANE

POWER PLANE

FOR HD AUDIO HEADER

Add 0805 short-pad  
03/18

VDDXL\_33  
WAKE ON LAN=>3.3V\_S5  
NONE=>3.3V\_S0

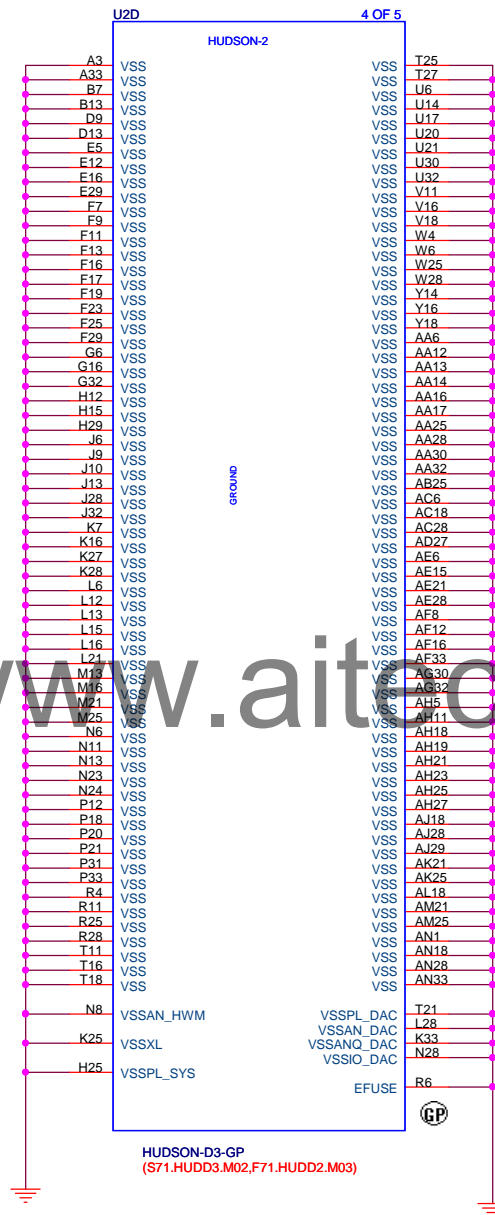
VDDPL\_11  
WAKE ON LAN=>1.1V\_S5  
NONE=>1.1V\_S0



Follow CRB, change to 2.2K  
02/21

```
Just EC Enable is different from AMD CRB
AMD: enable
```

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	RESERVED	Normal Refclk termination DEFAULT	USE RESERVED PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCIPLL	RESERVED	Inverted Refclk termination	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



TBD

www.aitech1.ru



Wistron Incorporated  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			Reserve
Size	Document Number	Rev	
B	Parker	-1	
Date:	Friday, May 13, 2011	Sheet	23 of 99

TBD

www.aitech1.ru




Wistron Incorporated  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			Reserve
Size	Document Number	Rev	
B	Parker	-1	
Date:	Friday, May 13, 2011	Sheet	24 of 99

TBD

www.aitech1.ru

		<b>Wistron Incorporated</b> 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title Reserve			
Size B	Document Number Parker		Rev -1
Date:	Friday, May 13, 2011	Sheet 25 of 99	

TBD


www.artech1.ru



Wistron Incorporated  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			Reserve
Size	Document Number	Rev	
B	Parker	-1	
Date:	Friday, May 13, 2011	Sheet	26 of 99

**TBD**  
[www.aitech1.ru](http://www.aitech1.ru)

		<b>Wistron Incorporated</b> 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title KBC			
Size B	Document Number Parker		Rev -1
Date:	Friday, May 13, 2011		Sheet 27 of 99

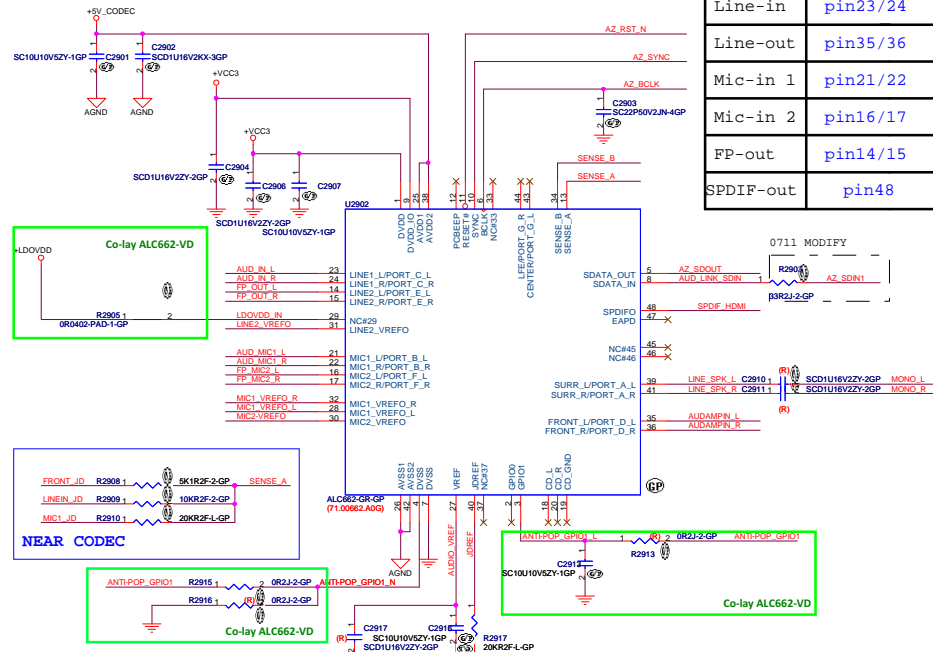
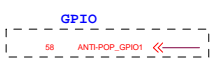
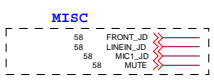
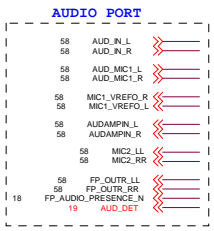
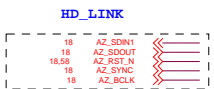
TBD

www.aitech1.ru

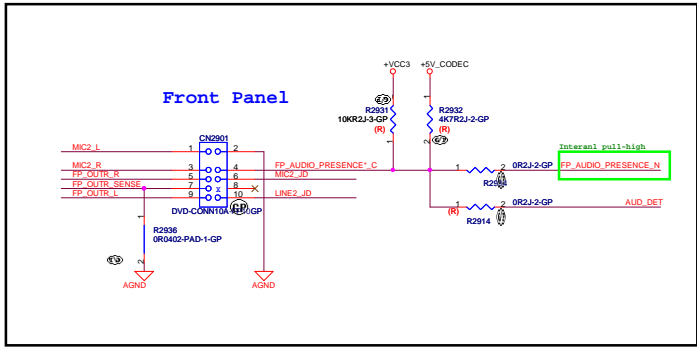
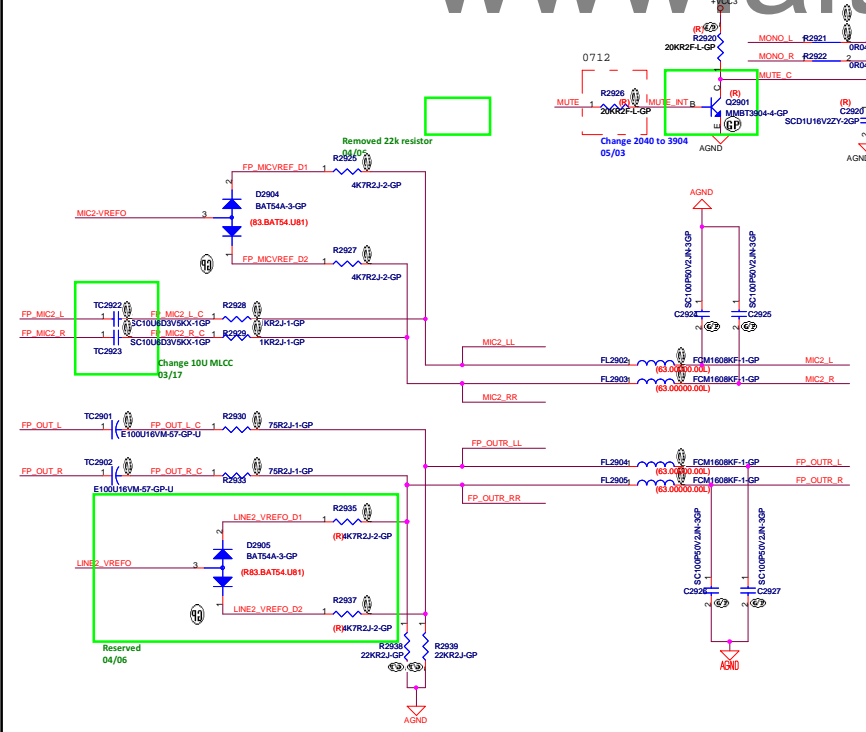
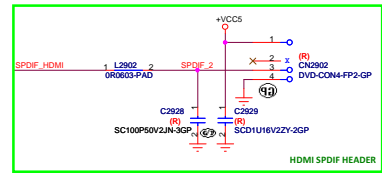
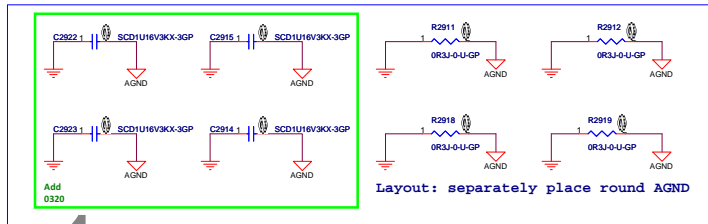
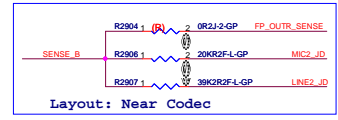
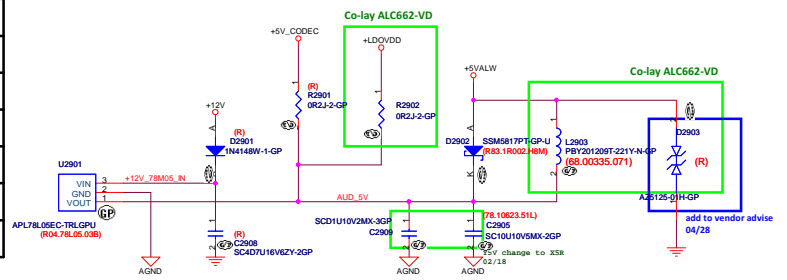


Wistron Incorporated  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			Thermal Chip	
Size	Document Number			Rev
B	Parker			-1
Date:	Friday, May 13, 2011	Sheet	28	of 99



Line-in	pin23/24
Line-out	pin35/36
Mic-in 1	pin21/22
Mic-in 2	pin16/17
FP-out	pin14/15
SPDIF-out	pin48



www.aitech1.ru

TBD


www.aitech1.ru



Wistron Incorporated  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei


Title			Audio AMP	
Size	Document Number			Rev
B	Parker			-1
Date:	Friday, May 13, 2011	Sheet	30	of 99

**TBD**  
[www.aitech1.ru](http://www.aitech1.ru)

		<b>Wistron Incorporated</b> 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title LOM			
Size B	Document Number Parker		Rev -1
Date:	Friday, May 13, 2011	Sheet	31 of 99

TBD

www.aitech1.ru

		<b>Wistron Incorporated</b> 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title Card Reader			
Size B	Document Number Parker		Rev -1
Date:	Friday, May 13, 2011		Sheet 32 of 99

TBD

www.aitech1.ru



Wistron Incorporated  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			1394
Size	Document Number		Rev
B	Parker		-1
Date:	Friday, May 13, 2011		Sheet 33 of 99

TBD

www.aitech1.ru



**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			Smart Card		
Size	Document Number				Rev
B	Parker				-1
Date:	Friday, May 13, 2011			Sheet	34 of 99

TBD


www.aitech1.ru



**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei


Title			USB3.0 Solution		
Size	Document Number				Rev
B	Parker				-1
Date:	Friday, May 13, 2011			Sheet	35 of 99

TBD  
www.aitech1.ru

		<b>Wistron Incorporated</b> 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title Power plan Enable			
Size B	Document Number Parker		Rev -1
Date:	Friday, May 13, 2011	Sheet	36 of 99


TBD

www.aitech1.ru

		<b>Wistron Incorporated</b> 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title		Adapter OCP Ccuit	
Size B	Document Number Parker		Rev -1
Date:	Friday, May 13, 2011		Sheet 37 of 99

TBD

www.aitech1.ru

		<b>Wistron Incorporated</b> 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title DCIN Jack			
Size B	Document Number Parker		Rev -1
Date:	Friday, May 13, 2011	Sheet 38 of 99	

TBD  
www.aitech1.ru

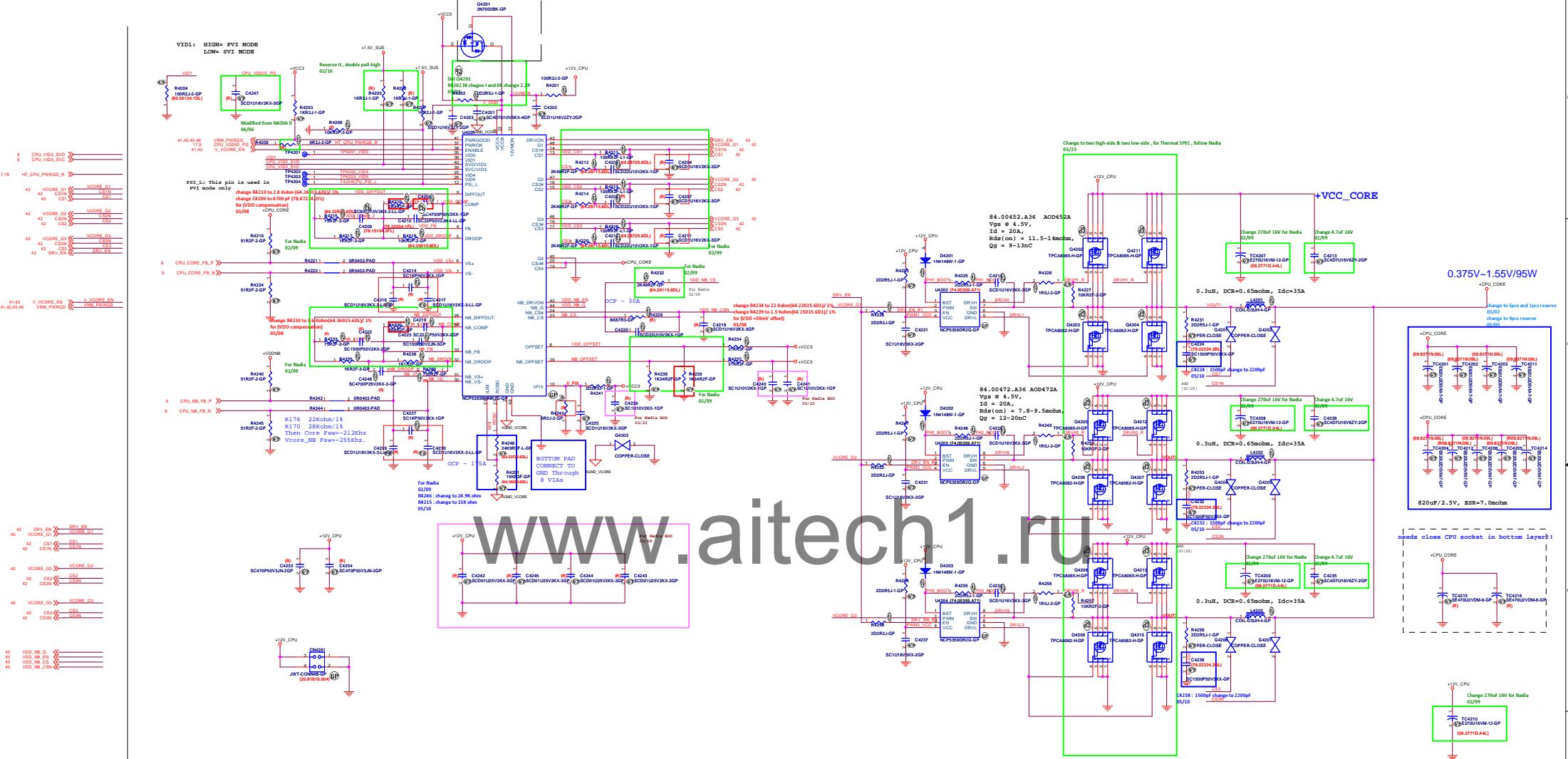


Wistron Incorporated  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			BATT CONN/DOCK DCIN		
Size	Document Number				Rev
B	Parker				-1
Date:	Friday, May 13, 2011		Sheet	39	of 99





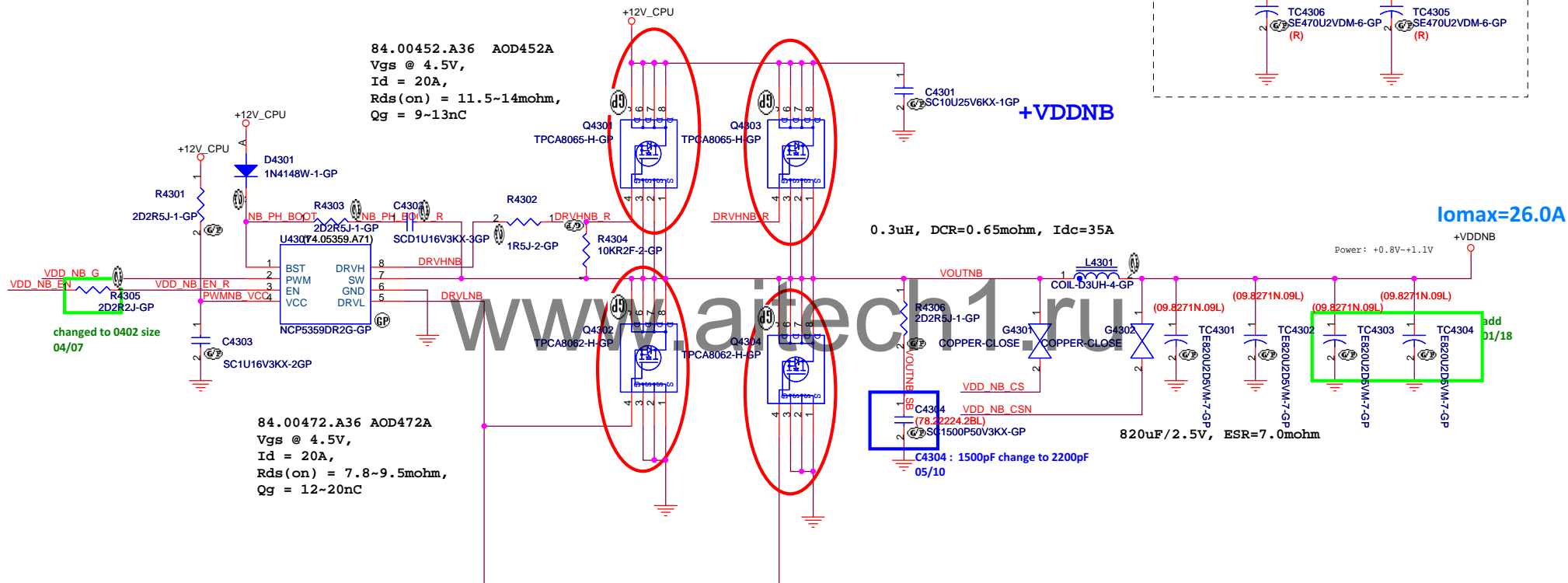
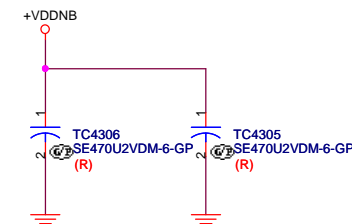


42 VDD\_NB\_G  
42 VDD\_NB\_EN  
42 VDD\_NB\_CS  
42 VDD\_NB\_CSN

84.00452.A36 AOD452A  
Vgs @ 4.5V,  
Id = 20A,  
Rds(on) = 11.5~14mohm,  
Qg = 9~13nC

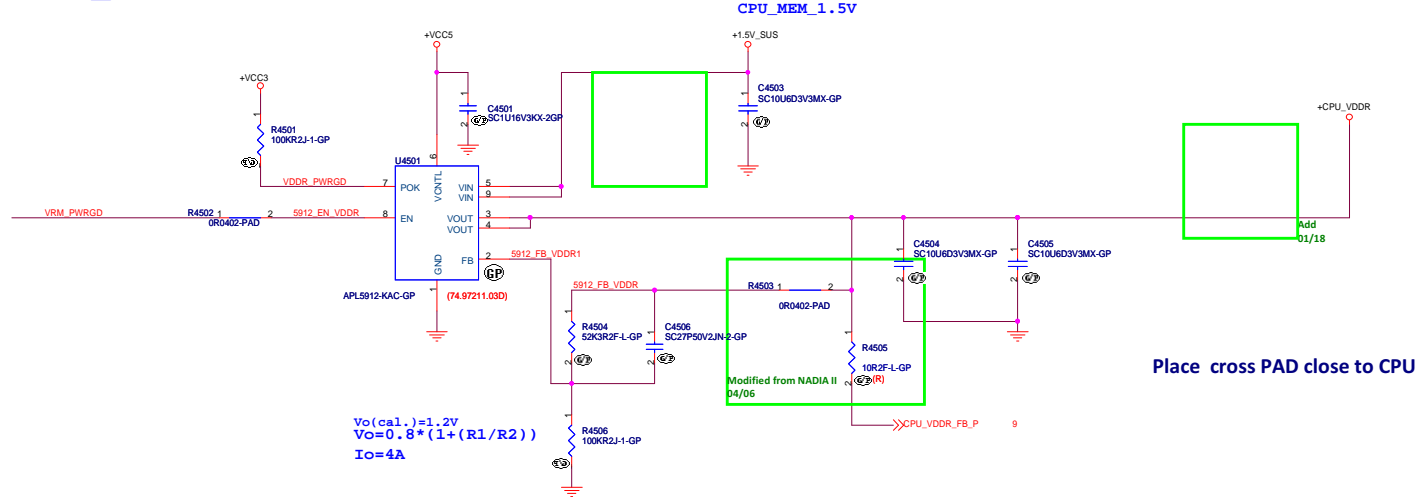
84.00472.A36 AOD472A  
Vgs @ 4.5V,  
Id = 20A,  
Rds(on) = 7.8~9.5mohm,  
Qg = 12~20nC

needs close CPU socket in top layer!!

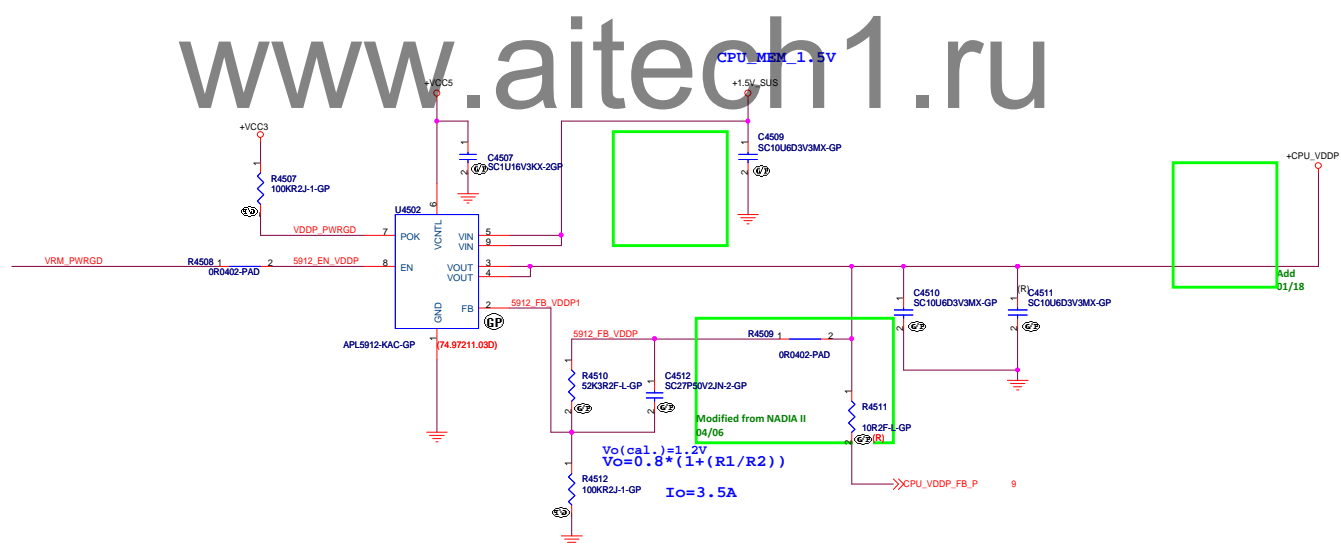




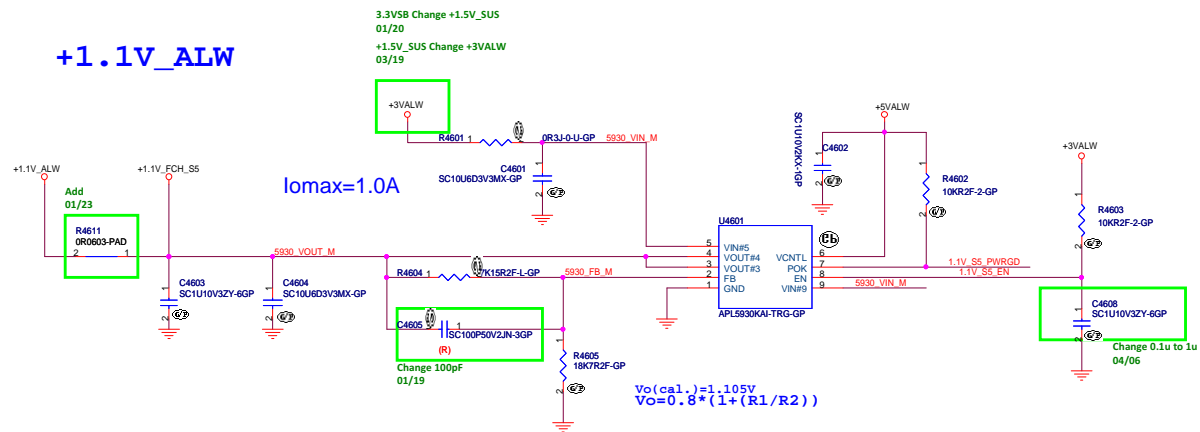
+CPU\_VDDR



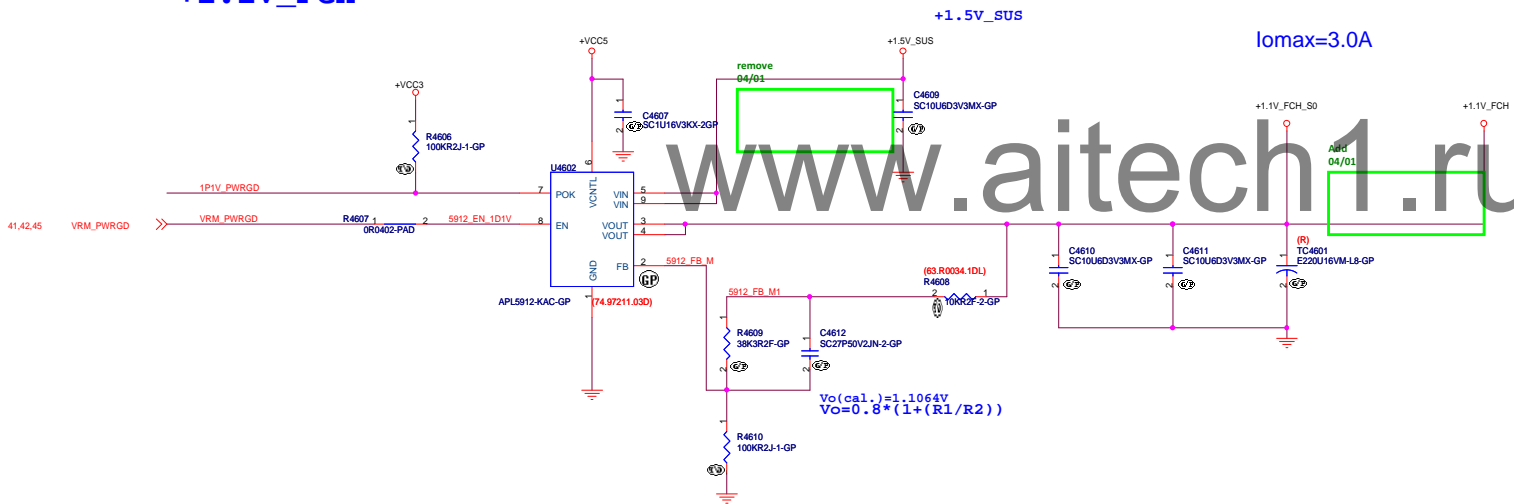
+CPU\_VDDP




## +1.1V\_ALW



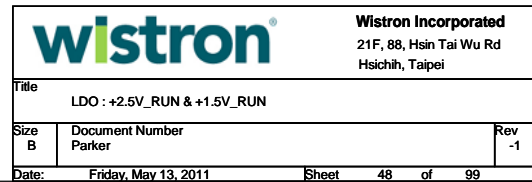
## +1.1V\_FCH



www.aitech1.ru


		<b>Wistron Incorporated</b> 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title LDO : +1.8V_RUN			
Size B	Document Number Parker		Rev -1
Date:	Friday, May 13, 2011	Sheet	47 of 99

$I_{\text{max}}=0.5\text{A}$

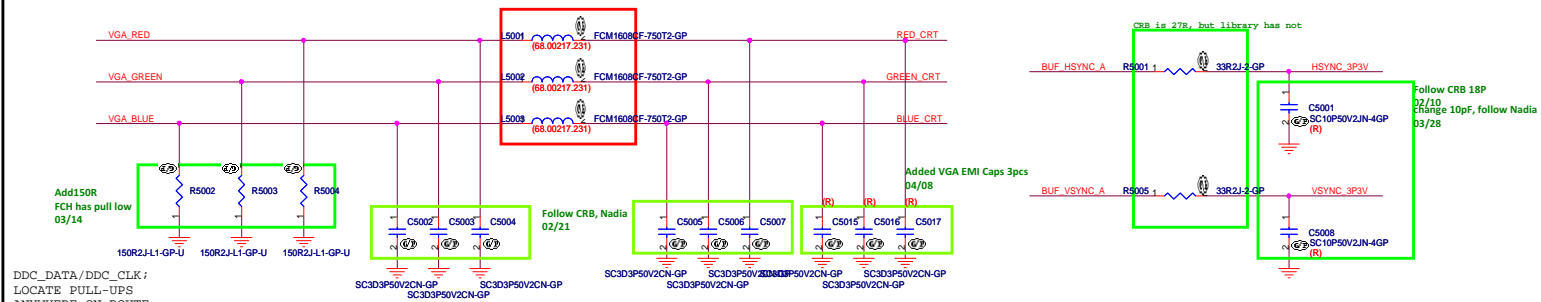
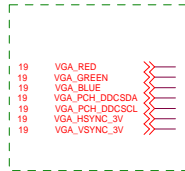


TBD

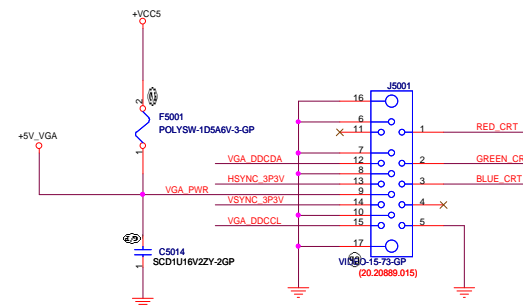
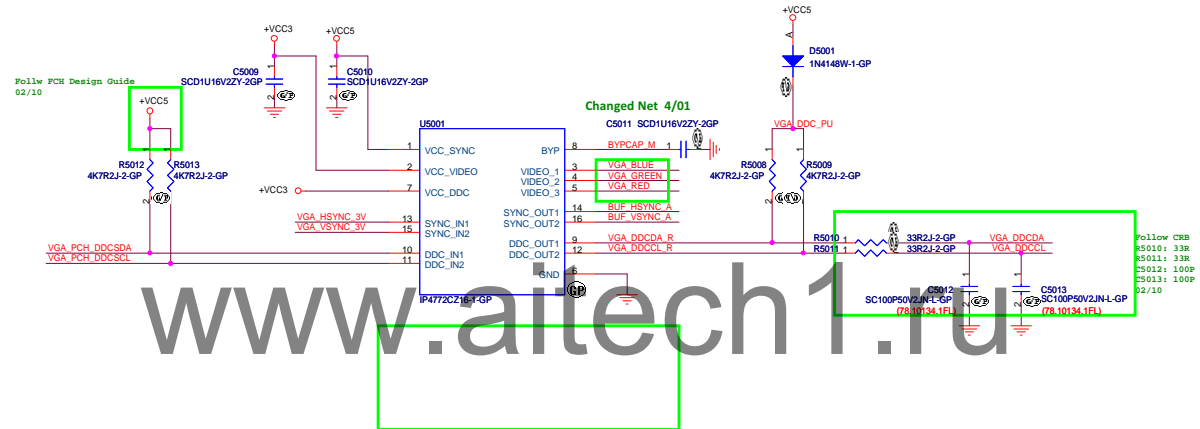
www.aitech1.ru

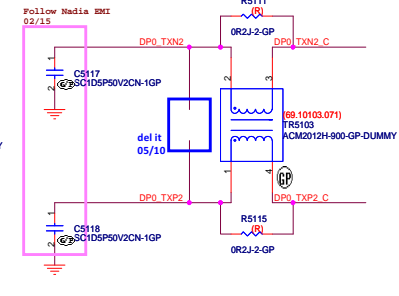
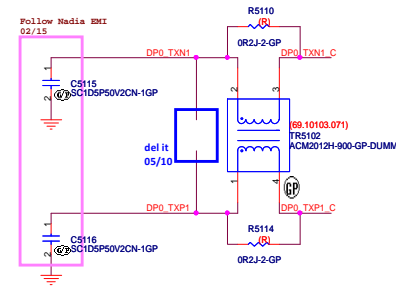
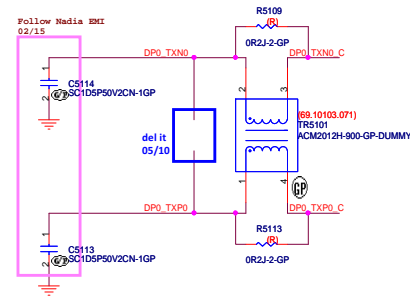
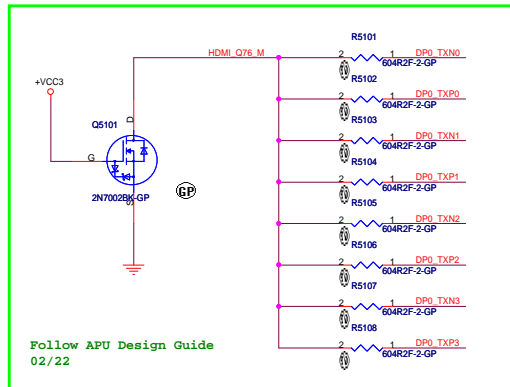
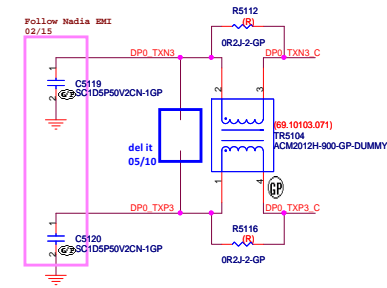
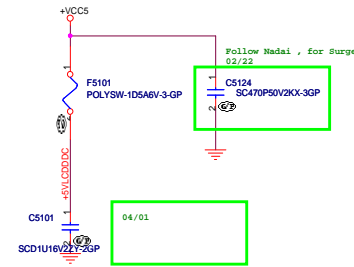
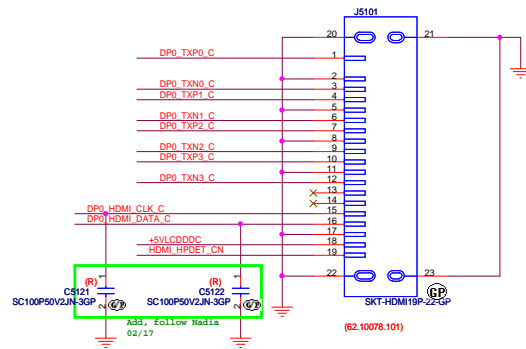
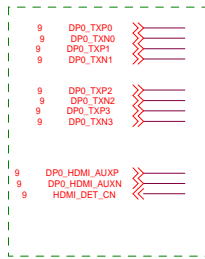
		<b>Wistron Incorporated</b> 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title LCD/Inverter Connector + Cam			
Size B	Document Number Parker		Rev -1
Date:	Friday, May 13, 2011		Sheet 49 of 99

DDC\_DATA/DDC\_CLK;  
LOCATE PULL-UPS  
ANYWHERE ON ROUTE  
OF TRACE



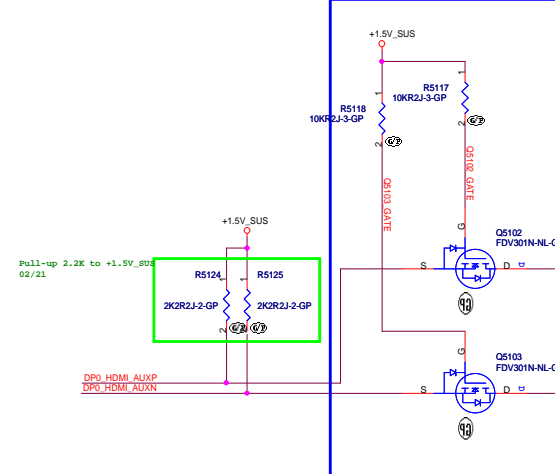
VGA ESD Parts change to this IC 6/18



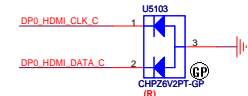
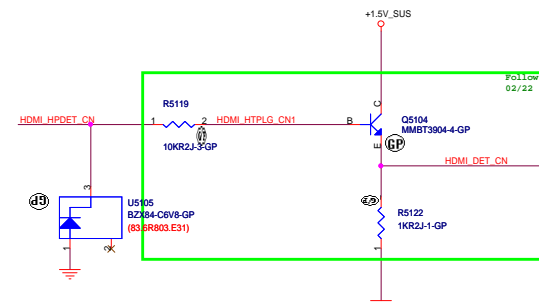
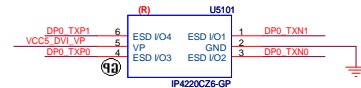
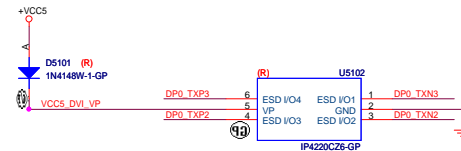
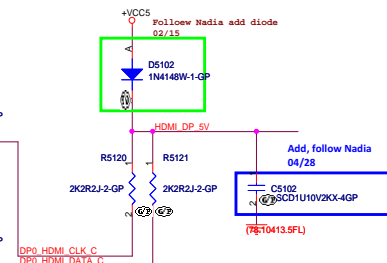


www.aitech1.ru

Q5102, Q5103 : 2N7002 change to 301N  
R5117 : change to 10K ohm  
MOS G-side Power Source change to +1.5V\_SUS  
04/28



Level shift



TBD


www.aitech1.ru



Wistron Incorporated  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			Display Port		
Size	Document Number				Rev
B	Parker				-1
Date:	Friday, May 13, 2011			Sheet	52 of 99

**TBD**  
[www.aitech1.ru](http://www.aitech1.ru)

		<b>Wistron Incorporated</b> 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title S-Video			
Size B	Document Number Parker		Rev -1
Date:	Friday, May 13, 2011	Sheet	53 of 99

**TBD**

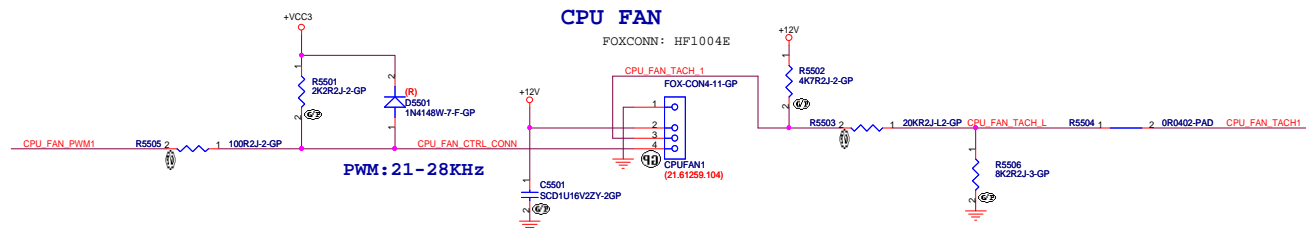
[www.aitech1.ru](http://www.aitech1.ru)



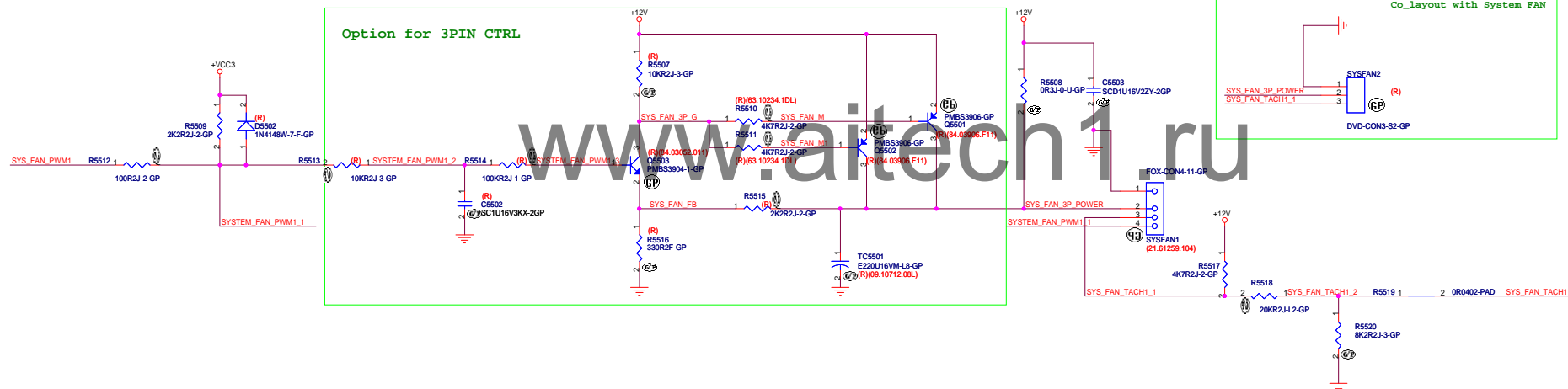
**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			DVI
Size	Document Number	Rev	
B	Parker	-1	
Date:	Friday, May 13, 2011	Sheet	54 of 99

78	CPU_FAN_TACH1	»»	_____
78	CPU_FAN_PWM1	»»	_____
78	SYS_FAN_TACH1	»»	_____
78	SYS_FAN_PWM1	»»	_____



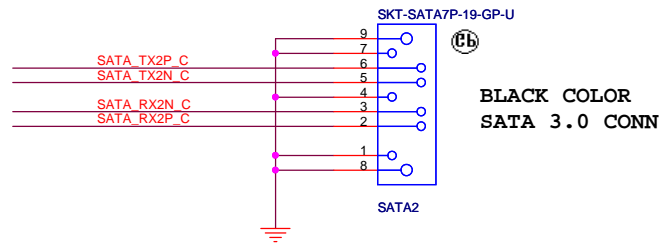
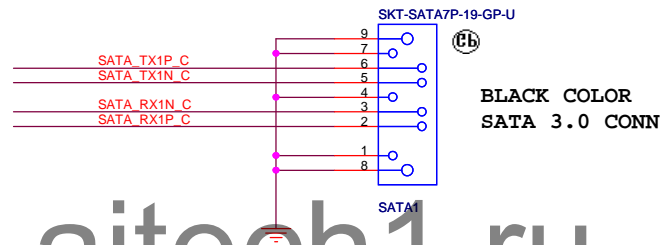
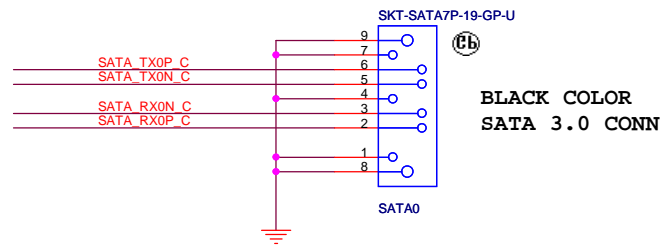
### Option for 3PIN CTRL



19 SATA\_TX0P\_C  
19 SATA\_TX0N\_C  
19 SATA\_RX0P\_C  
19 SATA\_RX0N\_C

19 SATA\_TX1P\_C  
19 SATA\_TX1N\_C  
19 SATA\_RX1P\_C  
19 SATA\_RX1N\_C

19 SATA\_TX2P\_C  
19 SATA\_TX2N\_C  
19 SATA\_RX2P\_C  
19 SATA\_RX2N\_C



www.aitech1.ru

TBD

www.aitech1.ru



**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title  
E-SATA + Re-driver IC

Size B	Document Number Parker	Rev -1
-----------	---------------------------	-----------

Date: Friday, May 13, 2011 Sheet 57 of 99

29 FP\_OUTR\_LL  
29 FP\_OUTR\_RR  
29 MIC2\_LL  
29 MIC2\_RR  
29 AUD\_IN\_L  
29 AUD\_IN\_R  
29 MIC1\_VREF0\_L  
29 AUD\_MIC1\_L  
29 AUD\_MIC1\_R  
29 MIC1\_VREF0\_R  
29 AUDAMPIN\_L  
29 AUDAMPIN\_R

29	LINEIN_ID	←←
29	FRONT_ID	←←
29	MIC1_ID	←←
29	AZ_RST_N	→→
29	ANTI-POP_GPIO1	→→
29	MUTE	←←
18	SPKR	→→

[illegible][illegible]

The diagram shows the PCB layout for the MIC IN (PINK) section. It includes the following components and connections:

- Microphone Input:** MIC1\_0, MIC1\_VREF0\_L, MIC1\_VREF0\_R, MIC1\_1L, MIC1\_1R, MIC1\_2L, MIC1\_2R.
- Resistors:** RS513 (2K2R2J-2-GP), RS514 (2K2R2J-1-GP), RS515 (2K2R2J-1-GP), RS516 (2K2R2J-1-GP), RS517 (2K2R2J-2-GP), RS518 (2K2R2J-2-GP).
- Capacitors:** CS5803 (1000000000K10G), CS5804 (1000000000K10G), CS5805 (1000000000K10G), CS5806 (1000000000K10G), CS5807 (1000000000K10G), CS5808 (1000000000K10G), CS5809 (1000000000K10G), CS5810 (1000000000K10G).
- Other Components:** Change 10u MLCC 0317, C5809 (1000000000K10G), C5810 (1000000000K10G).
- Connections:** MIC1\_0 to MIC1\_1L and MIC1\_1R; MIC1\_VREF0\_L to MIC1\_2L and MIC1\_2R; MIC1\_VREF0\_R to MIC1\_2L and MIC1\_2R; MIC1\_1L to MIC1\_2L; MIC1\_1R to MIC1\_2R; MIC1\_2L to MIC1\_2R.

NOTE:  
MIC GROUND ROUT BACK TO COBEC  
ALONG WITH MIC TRACE.  
THE MIC\_GND TO AGND NEAR CODEC

Removed 32k resistor  
04/06

Layout: PLACE NEAR CONN



BLUE  
LIME  
PINK

1K ohm change to 10K ohm  
05/04

BLUE

LIME

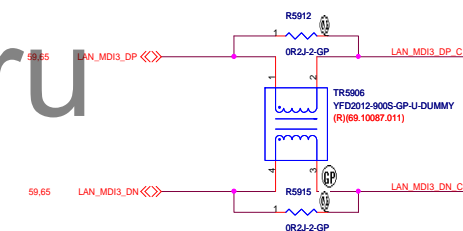
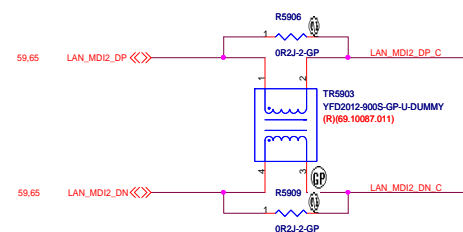
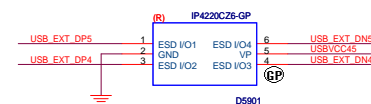
Change 3904 to 2040 04/06

[illegible][illegible][illegible]

The diagram shows a buzzer circuit connected to a microcontroller. The microcontroller's BZ\_ON pin is connected to the buzzer. The circuit includes a 2K2R2J-2-GP resistor, a 1K2J-1-GP resistor, and a 75R31-L-GP resistor. The buzzer is labeled BZ5801 and BUZZER-17-GPU. The microcontroller is powered by a 5VDC supply.



R5902 change to 100K ohm  
R5903 change to 150K ohm  
to fix leakage current



TBD

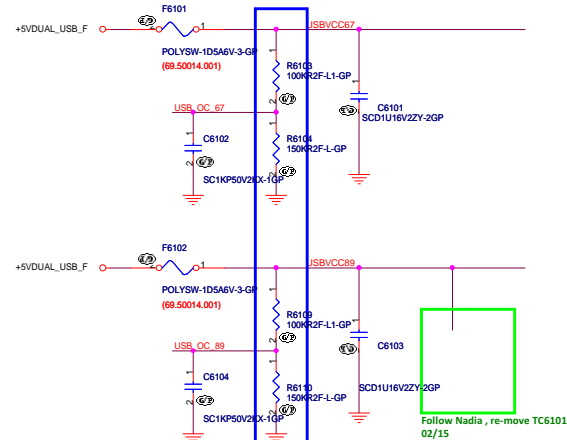
www.aitech1.ru



**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			Flash (KBC + PCH)/RTC
Size	Document Number	Rev	
B	Parker	-1	
Date:	Friday, May 13, 2011	Sheet	60 of 99

59 USB\_EXT\_DN0 << >> \_\_\_\_\_  
59 USB\_EXT\_DP0 \_\_\_\_\_  
59 USB\_EXT\_DN1 << >> \_\_\_\_\_  
59 USB\_EXT\_DP1 \_\_\_\_\_



+5VDUAL\_USB\_F

F6103

POLYSW-1D5A6V-3-GP  
(69.50014.001)

USBVCC01

R6115  
100KR2F-L1-GP

C6105

SCD1U16W2ZY-2GP

remove TC6102  
3/26

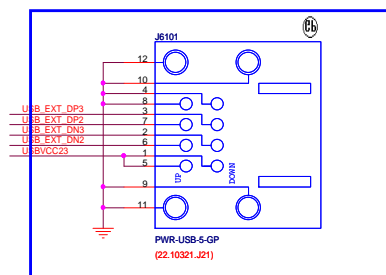
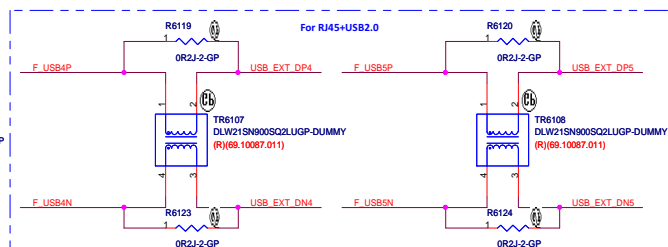
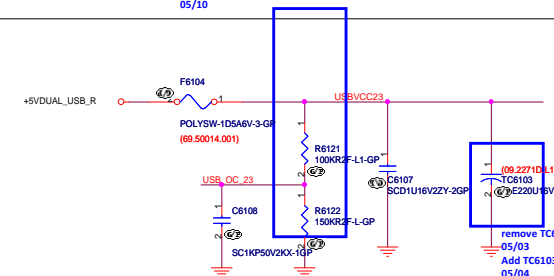
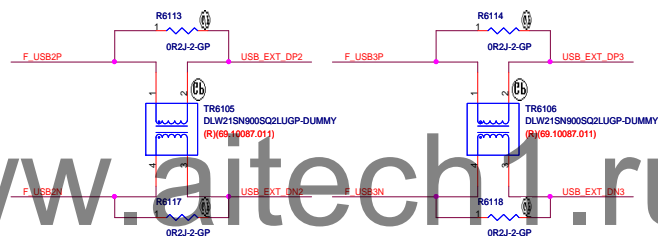
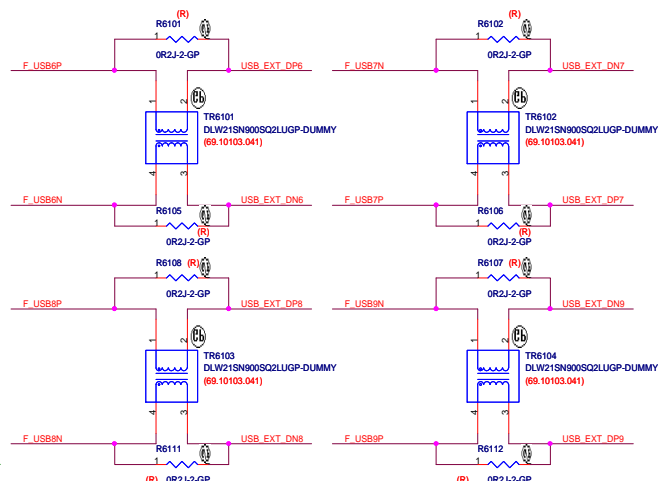
R6116  
50KR2F-L1-GP

USB\_OC\_01

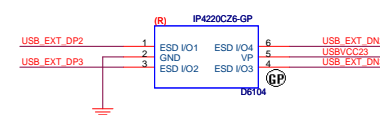
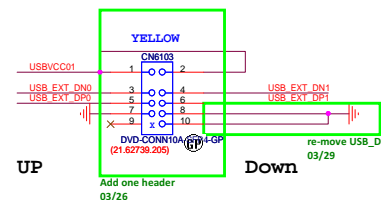
C6106

SC1KP50 2KX-1GP

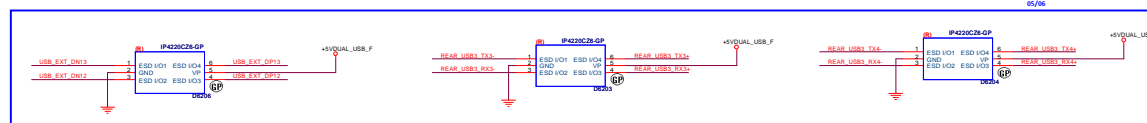
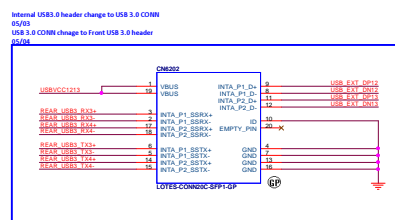
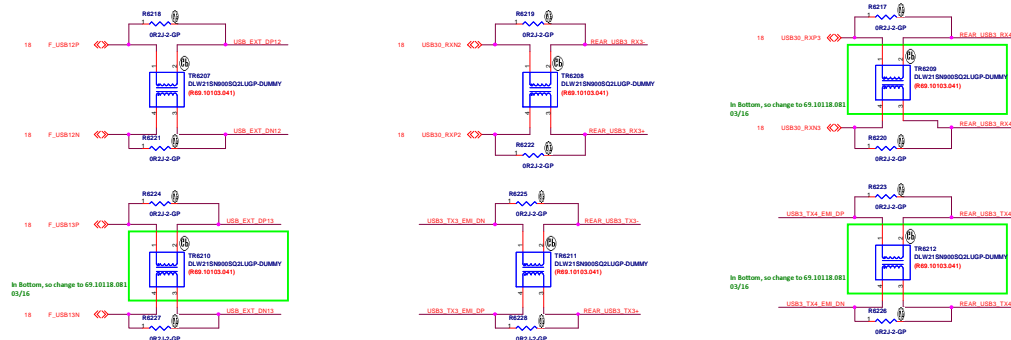
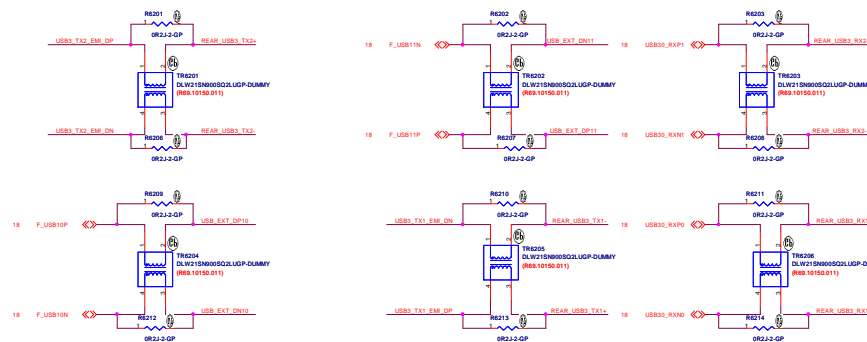
R6103, R6109, R6115, R6121 change to 100K ohm  
R6104, R6110, R6116, R6122 change to 150K ohm  
to fix leakage current  
05/10



Rear USB2.0 CONN change to Front USB2.0 header  
05/03  
Front USB 2.0 header change to Rear USB 2.0 CONN  
05/04



## USB 3.0 Front Header



**TBD**  
[www.aitech1.ru](http://www.aitech1.ru)



**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			Bluetooth	
Size	Document Number			Rev
B	Parker			-1
Date:	Friday, May 13, 2011		Sheet	63 of 99

TBD

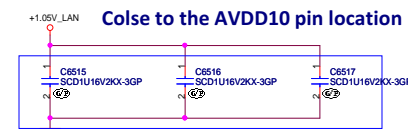
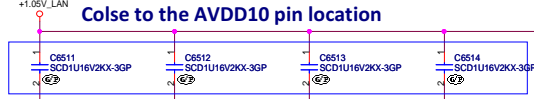
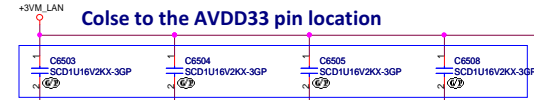
www.aitech1.ru



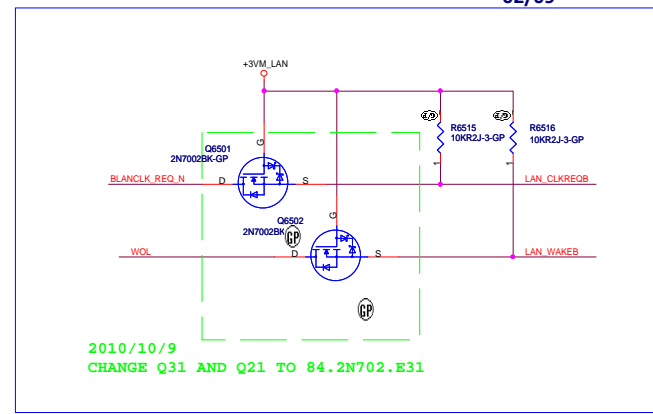
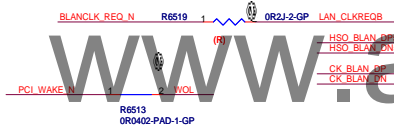
**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			Finger Printer Connector		
Size	Document Number				Rev
B	Parker				-1
Date:	Friday, May 13, 2011			Sheet	64 of 99

# 2010/10/8 LAN POWER CHANGE TO V\_3P3\_DUAL




2010/10/12  
No support ASF2.0, Set it to NC




**Layout close to FCH 02/09**

<b>wistron</b>		<b>Wistron Incorporated</b>	
Realtek Gb LAN-RTL8111E		21F, 88, Sec.1, Hsin Tai Wu Rd	
File		Haichih, Taipei Hsein	
Size	C	Document Number	Rev
Date:	Tuesday, June 07, 2011	Sheet	65 of 99

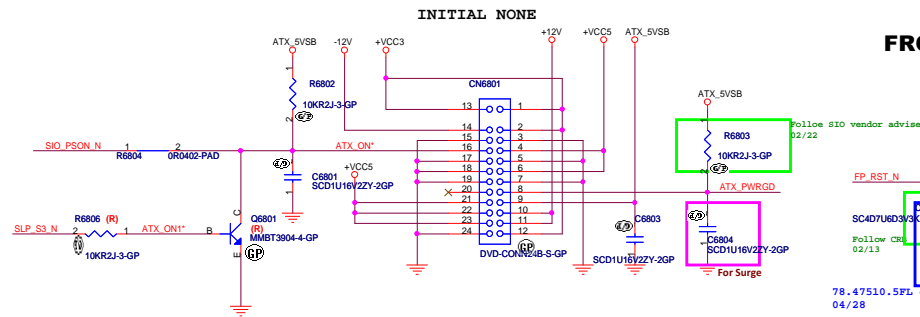
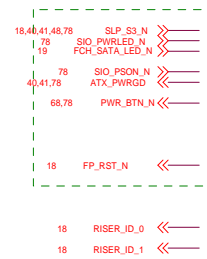
**TBD**  
[www.aitech1.ru](http://www.aitech1.ru)

		<b>Wistron Incorporated</b> 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title WWAN CONN/SIM Socket			
Size B	Document Number Parker		Rev -1
Date:	Friday, May 13, 2011	Sheet	66 of 99

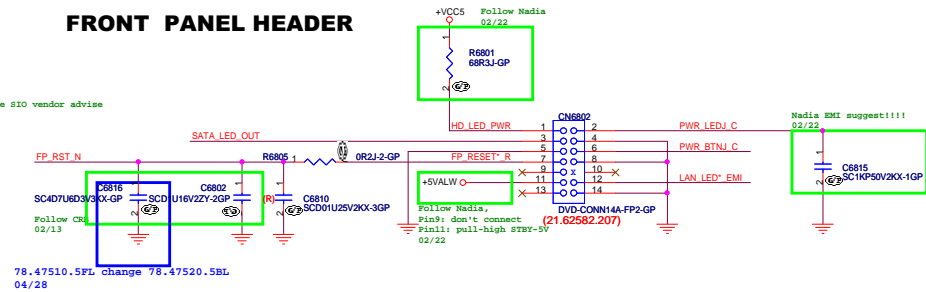
**TBD**  
[www.aitech1.ru](http://www.aitech1.ru)

		<b>Wistron Incorporated</b> 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title 3rd MINICARD			
Size B	Document Number Parker		Rev -1
Date:	Friday, May 13, 2011		Sheet 67 of 99

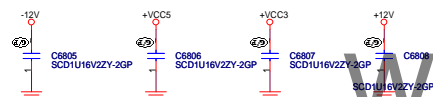
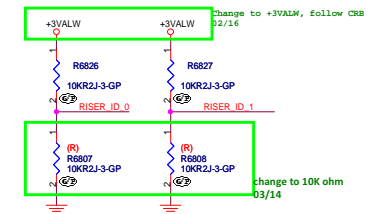
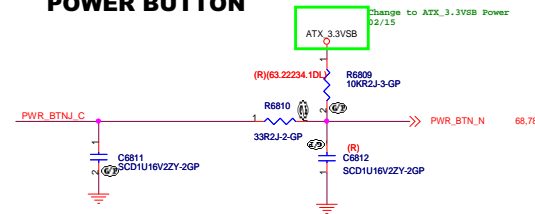
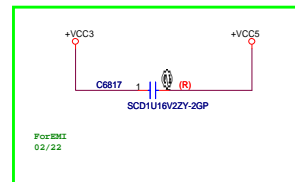
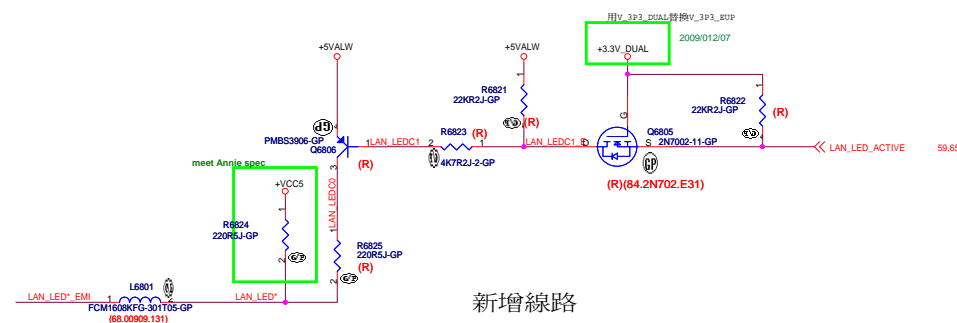
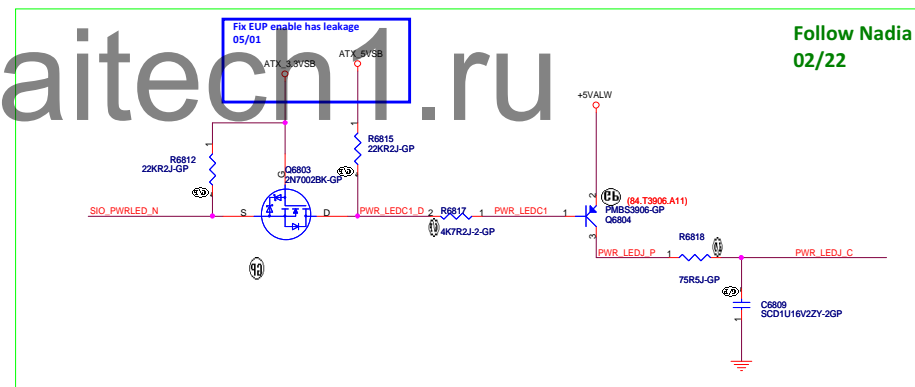
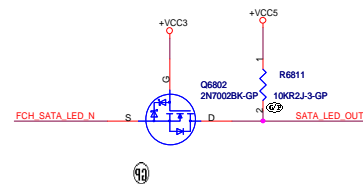
## ATX CONNECTOR



## FRONT PANEL HEADER

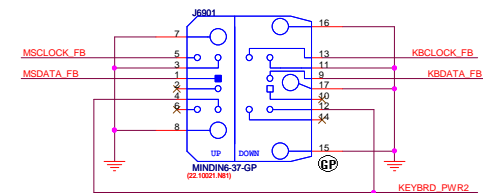
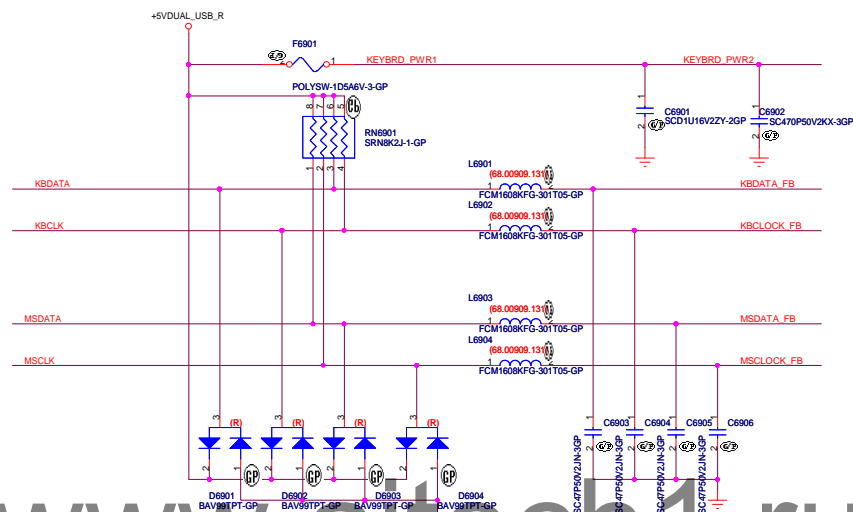


## POWER BUTTON

**HDD LED**

新增線路

78 KBDATA  
78 KBCLK  
78 MSDATA  
78 MSCLK



www.altech1.ru

TBD

www.aitech1.ru



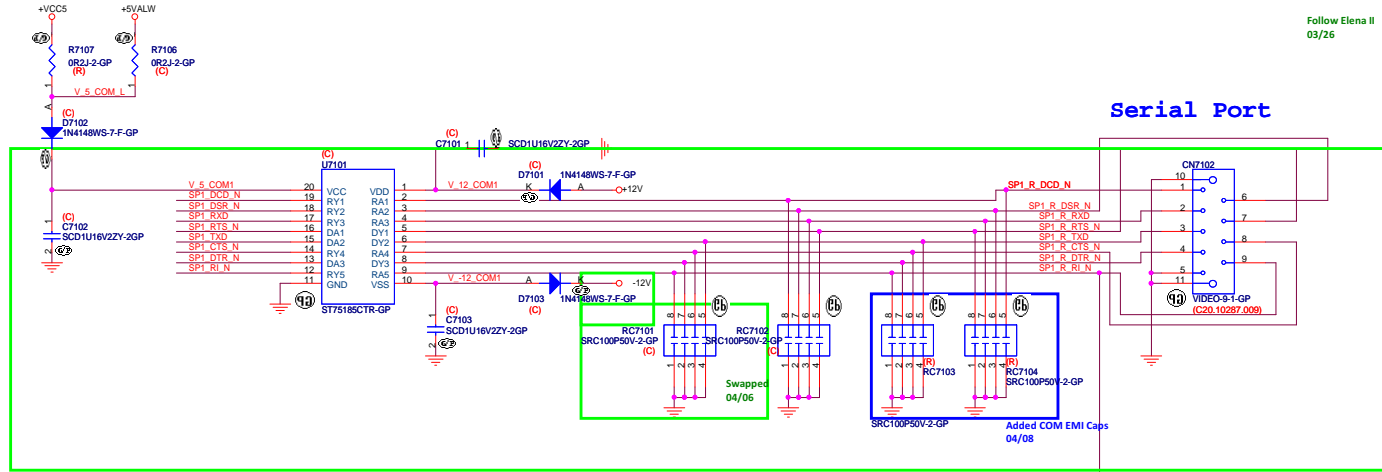
Wistron Incorporated  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			Hall Sensor	
Size	Document Number			Rev
B	Parker			-1
Date:	Friday, May 13, 2011		Sheet	70 of 99

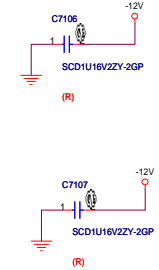
# SERIAL PORT

## COM Port

78 SPI1\_RTS\_N  
78 SPI1\_DTR\_N  
78 SPI1\_DSR\_N  
78 SPI1\_RXD\_N  
78 SPI1\_TXD\_N  
78 SPI1\_CTS\_N  
78 SPI1\_RI\_N



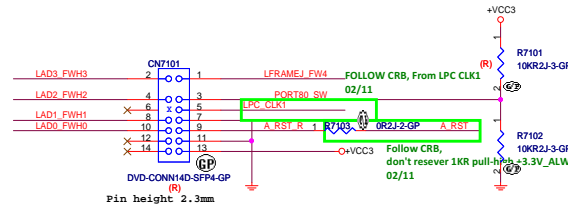
## Serial Port



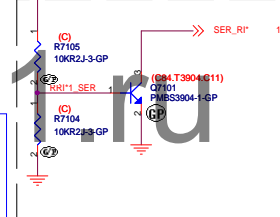
## Layout Close SIO


## LPC DEBUG PORT

17.78 LAD0\_FWH0  
17.78 LAD1\_FWH1  
17.78 LAD2\_FWH2  
17.78 LAD3\_FWH3  
17.78 LFRAMEJ\_FW4  
17.78 A\_RST  
17.21 LPC\_CLK1



## 20110525 Add for wake on modem ring



		<b>Wistron Incorporated</b> 21F, 8B, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>Serial Port/JTAG/Debug Port</b>			
Size C	Document Number <b>Parker</b>		Rev -1
Date:	Wednesday, June 08, 2011	Sheet	71 of 99

TBD

www.aitech1.ru



**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			RJ11+MDC
Size	Document Number	Rev	
B	Parker	-1	
Date:	Friday, May 13, 2011	Sheet	72 of 99

TBD

www.aitech1.ru



**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			1394 CONN
Size	Document Number	Rev	
B	Parker	-1	
Date:	Friday, May 13, 2011	Sheet	73 of 99

TBD

www.aitech1.ru



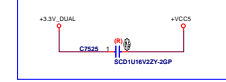
**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			Card Reader Connector		
Size	Document Number				Rev
B	Parker				-1
Date:	Friday, May 13, 2011			Sheet	74 of 99

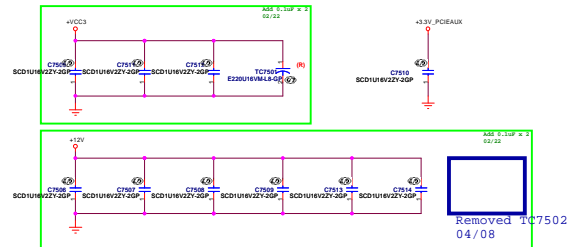
# Layout Colse to PCI-e 02/23



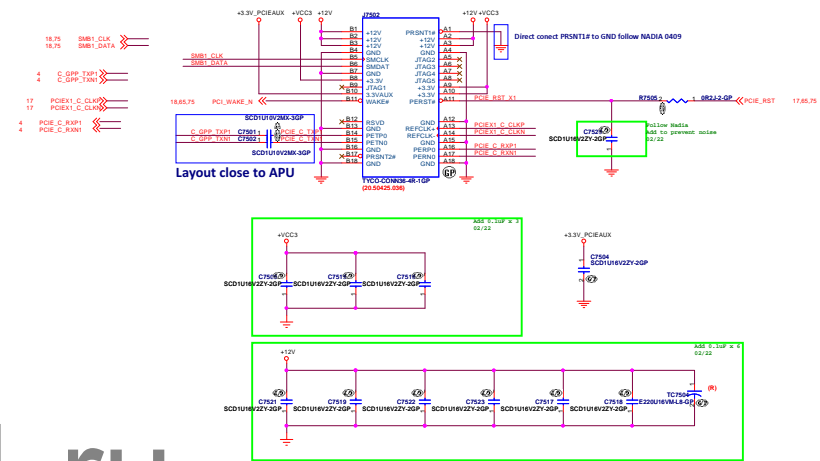
# Cross Moat MLCC, close to TC7504



T.CONN104-484-GP  
(01.00016.104)  
Change to has latch slot  
04/08



# PCIEX1 CONN



www.aitech1.ru

TBD

www.aitech1.ru



Wistron Incorporated  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			Smart Card Socket	
Size	Document Number			Rev
B	Parker			-1
Date:	Friday, May 13, 2011		Sheet	76 of 99

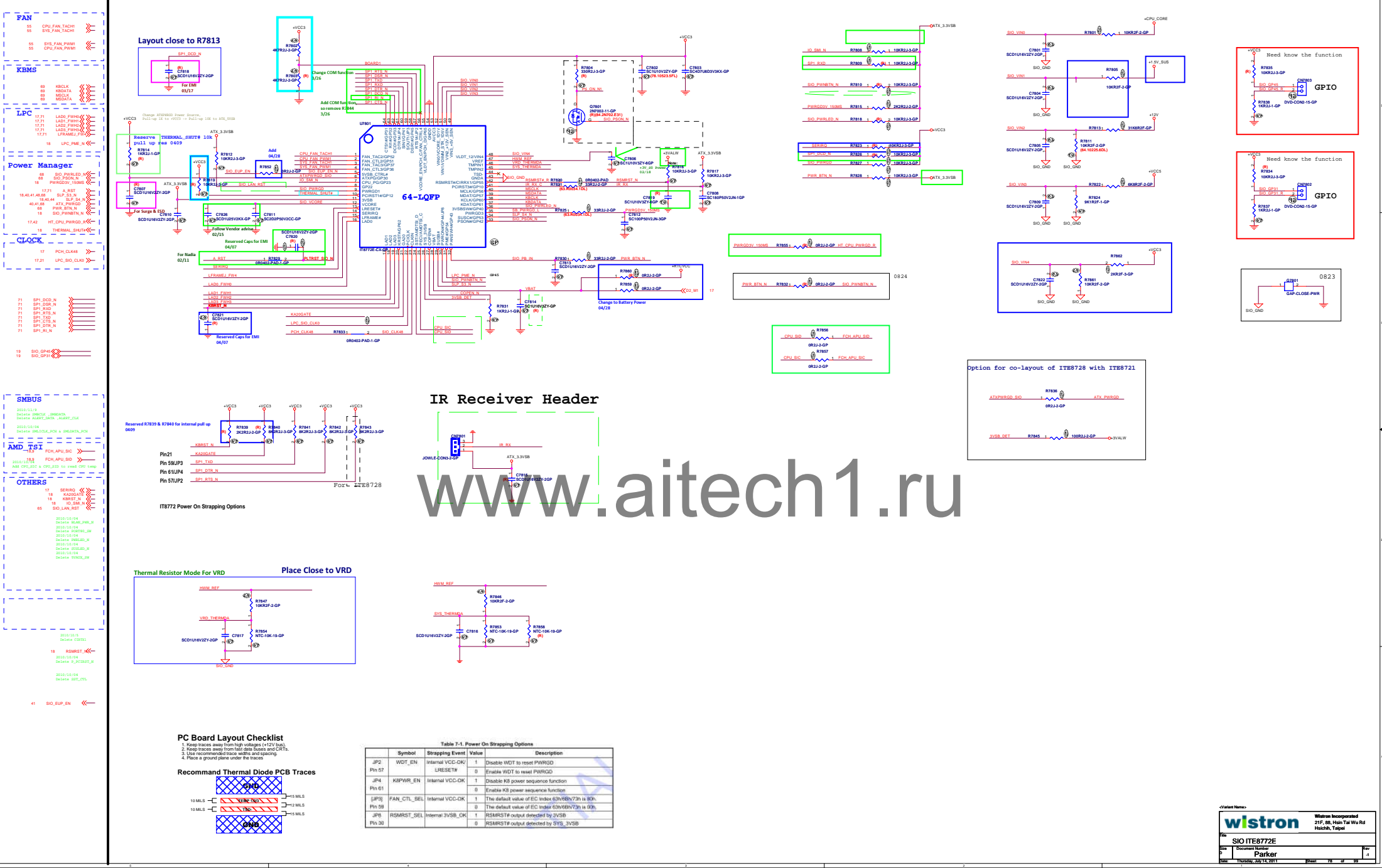
TBD

www.aitech1.ru



Wistron Incorporated  
21F, 88, Sec.1,Hsin Tai Wu Rd  
Hsichih, Taipei Hsien

Title			TPM
Size	Document Number	Rev	
B	Parker	-1	
Date:	Friday, May 13, 2011	Sheet	77 of 99



PC Board Layout Checklist

- 1. Keep traces away from high voltages (+12V bus).
- 2. Keep traces away from hot die nodes and CRTs.
- 3. Use recommended trace widths and spacing.
- 4. Place a ground plane under the traces.

Recommend Thermal Diode PCB Traces

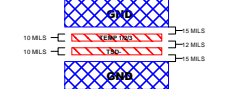


Table 7-1. Power On Strapping Options

Symbol	Strapping Event	Value	Description
JP2	WDT_EN	Internal VCC-OK	1 Disable WDT to reset PWRGD
Pin 57	LRESETW	0	Enable WDT to reset PWRGD
JP4	KBPWR_EN	Internal VCC-OK	1 Disable KB power sequence function
Pin 51			0 Enable KB power sequence function
JP5	FAN_CTL_SEL	Internal VCC-OK	1 The default value of EC input 53kΩ/60kΩ is 53kΩ.
Pin 58			0 The default value of EC input 53kΩ/60kΩ is 60kΩ.
JP6	RSRST_SEL	Internal V3VB OK	1 RSRST output detected by V3VB
Pin 30			0 RSRST output detected by SYS_V3VB

TBD

www.aitech1.ru



**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title  
G-Sensor (Reserve)

Size  
B

Document Number  
Parker

Rev  
-1

Date: Friday, May 13, 2011

Sheet 79 of 99

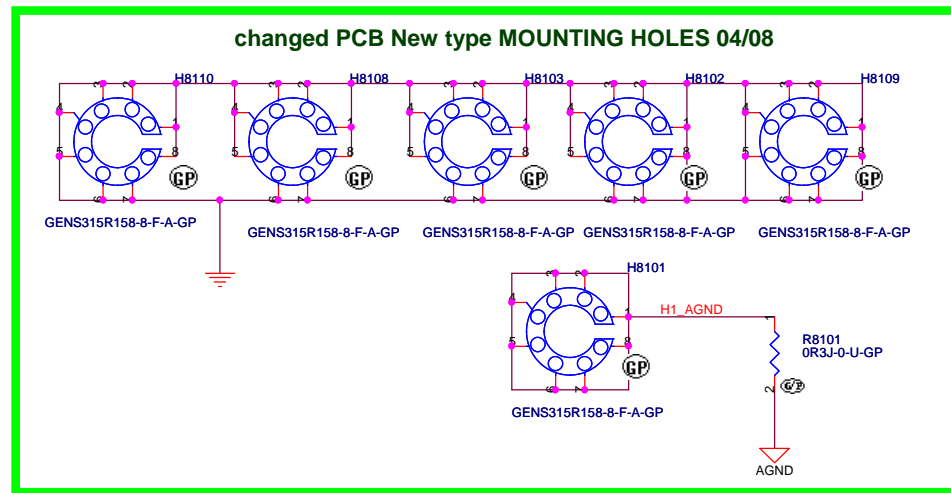
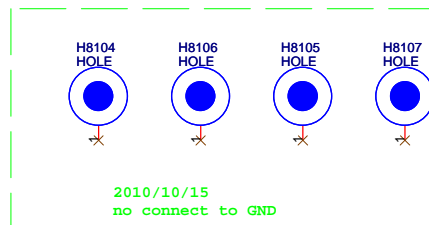
TBD

www.aitech1.ru

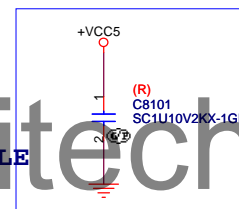


Wistron Incorporated  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			Reserve (RF/Other)	
Size	Document Number		Rev	
B	Parker		-1	
Date:	Friday, May 13, 2011		Sheet	80 of 99



Follow Nadia ESD  
Layout Close to ATX\_12V4201 of HOLE  
02/23



**wistron**

**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title  
Screw Holes, Springs, BOSS

Size B Document Number  
Parker

Rev  
-1

Date: Friday, May 13, 2011

Sheet 81 of 99

TBD

www.aitech1.ru



Wistron Incorporated  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			IO Board Connector (Reserve)	
Size	Document Number			Rev
B	Parker			-1
Date:	Friday, May 13, 2011		Sheet	82 of 99

TBD


www.aitech1.ru




**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			Discrete GPU (PEG/Strapping)		
Size	Document Number				Rev
B	Parker				-1
Date:	Friday, May 13, 2011		Sheet	83	of 99

**TBD**  
[www.aitech1.ru](http://www.aitech1.ru)


		<b>Wistron Incorporated</b> 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title Discrete GPU (Memory)			
Size B	Document Number Parker		Rev -1
Date:	Friday, May 13, 2011	Sheet 4	84 of 99

**TBD**  
[www.aitech1.ru](http://www.aitech1.ru)

		<b>Wistron Incorporated</b> 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title Discrete GPU (DP/LVDS/CRT/GP)			
Size B	Document Number Parker		Rev -1
Date:	Friday, May 13, 2011	Sheet	85 of 99

TBD

www.aitech1.ru

		<b>Wistron Incorporated</b> 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title Discrete GPU (Core Power)			
Size B	Document Number Parker		Rev -1
Date:	Friday, May 13, 2011	Sheet	86 of 99

TBD  
www.altech1.ru



**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			Discrete GPU (DPPWR/GND)		
Size	Document Number				Rev
B	Parker				-1
Date:	Friday, May 13, 2011			Sheet	87 of 99

TBD

www.aitech1.ru



**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			1st and 2nd VRAM chips		
Size	Document Number				Rev
B	Parker				-1
Date:	Friday, May 13, 2011			Sheet	88 of 99

TBD

www.aitech1.ru



**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			3rd and 4th VRAM chips		
Size	Document Number				Rev
B	Parker				-1
Date:	Friday, May 13, 2011			Sheet	89 of 99

TBD

www.aitech1.ru



Wistron Incorporated  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			5th and 6th VRAM chips		
Size	Document Number				Rev
B	Parker				-1
Date:	Friday, May 13, 2011			Sheet	90 of 99

TBD

www.aitech1.ru



**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title		
7rd and 8th VRAM chips		
Size	Document Number	Rev
B	Parker	-1
Date:	Friday, May 13, 2011	Sheet 91 of 99

TBD

www.aitech1.ru



**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			GPU Core Power		
Size	Document Number				Rev
B	Parker				-1
Date:	Friday, May 13, 2011			Sheet	92 of 99

TBD

www.aitech1.ru



Wistron Incorporated  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			GPU Other Power		
Size	Document Number				Rev
B	Parker				-1
Date:	Friday, May 13, 2011		Sheet	93	of 99

TBD

www.aitech1.ru



**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			Switchable GFX (1/2)
Size	Document Number	Rev	
B	Parker	-1	
Date:	Friday, May 13, 2011	Sheet	94 of 99

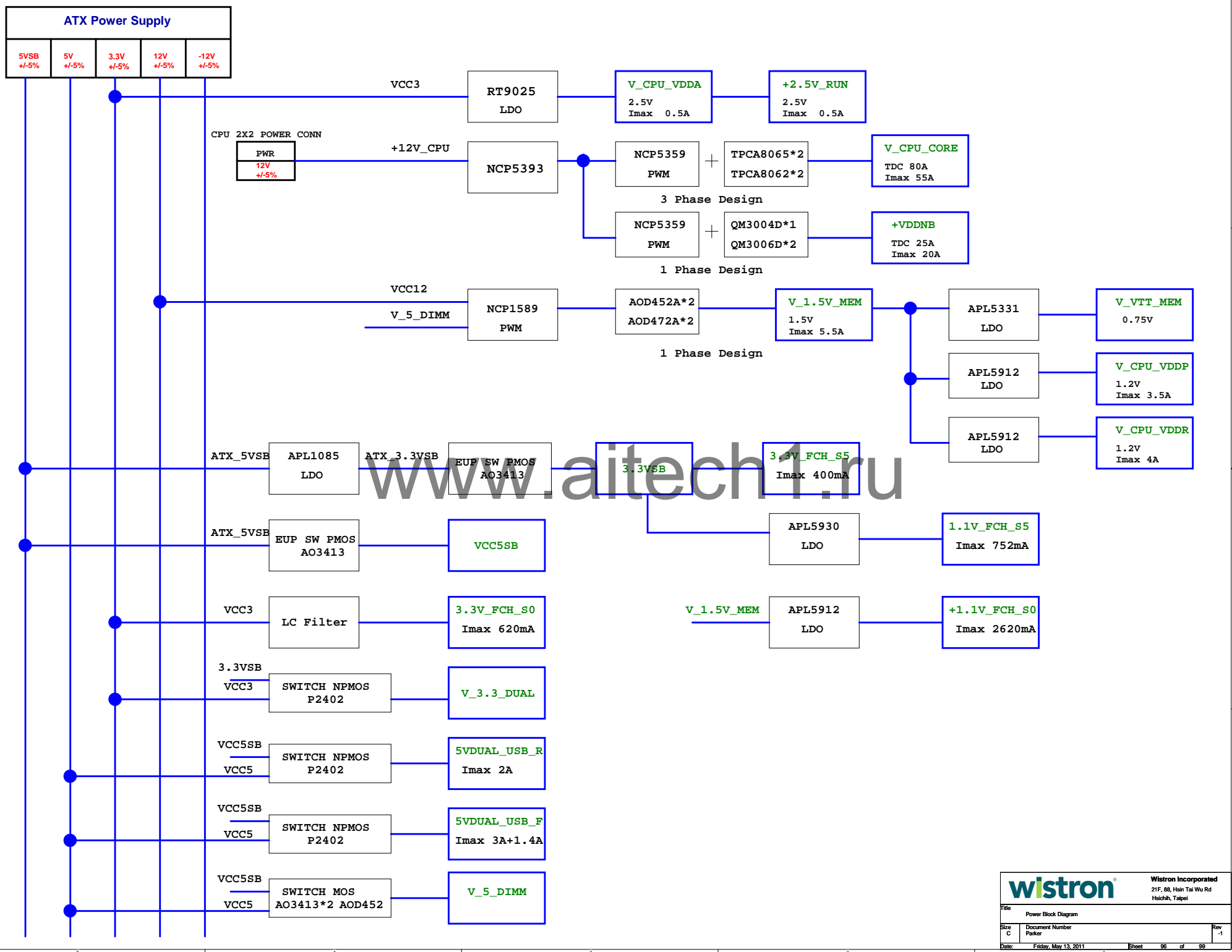
TBD

www.aitech1.ru



**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			Switchable GFX (2/2)
Size	Document Number	Rev	
B	Parker	-1	
Date:	Friday, May 13, 2011	Sheet	95 of 99



TBD

www.aitech1.ru



**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			SMBus Block Diagram		
Size	Document Number				Rev
B	Parker				-1
Date:	Friday, May 13, 2011			Sheet	97 of 99

TBD

www.aitech1.ru



**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			Thermal Block Diagram/Audio	
Size	Document Number			Rev
B	Parker			-1
Date:	Friday, May 13, 2011		Sheet	98 of 99

www.aitech1.ru



**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title			Chang History	
Size	Document Number			Rev
B	Parker			SA
Date:	Friday, May 13, 2011		Sheet	99 of 99